MIPS
by Imagination

MIPSfpga

One-day Workshops
Harvey Mudd College, Claremont, Ca., USA
13th & 14th May 2015

XILINX
UNIVERSITY PROGRAM

Free
SoC
Linux
FPGA
Verilog
Soft cores
Embedded

To: Teachers and Graduate Students interested in Computer Architecture and SOC Design

MIPSfpga is a 32-bit MIPS RISC soft-core processor optimized for running on low-cost FPGA platforms. It is non-obfuscated and a verified configuration of the popular MIPS microAptiv CPU found in many embedded devices; including the widely-used PIC32MZ microcontroller from Microchip. This workshop will show you how to use this core as part of a Computer Architecture course, paving the way for your students to use it in their projects, creating their own "SoC" designs. We are rolling out MIPSfpga together with comprehensive materials that make it easy to get started.

Our trainers will be Prof. Sarah Harris (UNLV), co-author of 'Digital Design & Computer Architecture' (Morgan Kaufman), and Parimal Patel, Principal Trainer and Content Developer for the Xilinx University Program.

By attending, you can be among the first to access MIPSfpga ahead of its global release in June!

Details & How To Apply: www.imgtec.com/MIPSfpga

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