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Сравнения MIPS и ARM для случая MIPSfpga / MIPS microAptiv UP

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Преимущество MIPS M14K против ARM Cortex-M3

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MicroMIPS Crams Code

New Processor Cores Introduce Denser 16/32-Bit Instruction Set

By Tom R. Halfhill (11/16/09-01)

Smaller is usually better for embedded processors, so MIPS Technologies is slimming down its 1980s-vintage instruction-set architecture. A new set of 16- and 32-bit instructions—dubbed microMIPS—uses less memory than existing 32-bit MIPS instructions and the 16-bit extensions added in the 1990s.

MicroMIPS will debut early next year in two new embedded-processor cores, the MIPS32 M14K and MIPS32 M14Kc. The M14K is an improvement on the MIPS32 M4K processor, introduced in 2002. It's a relatively simple, cacheless core intended for 32-bit microcontrollers in automobiles, industrial machinery, consumer electronics, and office equipment.

Its bigger brother, the M14Kc, is an improvement on the MIPS32 4KEc processor, introduced in 2003. The M14Kc has an MMU with a translation lookaside buffer (TLB), making it suitable for sophisticated embedded operating systems that manage virtual memory. It's designed for advanced consumer electronics, including DTVs, DVD players, set-top boxes, home networking equipment, personal entertainment devices, and digital cameras. Figure 1 shows how the M14K and M14Kc fit into the MIPS product line.

Both new processors respond much faster to interrupts and have better debugging features than the MIPS cores they supersede. Both gain advantages in clock speed, power consumption, and core size when compared with ARM's Cortex-M3 and ARM926 processors, and they give ARM's new Cortex-A5 a run for the money.

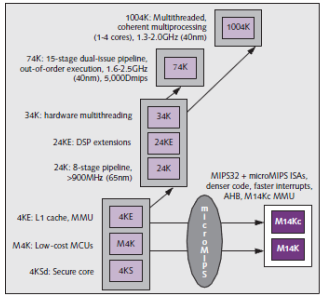


Figure 1. The new MIPS32 M14K and MIPS32 M14Kc processor cores introduce the microMIPS 16/32-bit instruction set and anchor the lower end of the MIPS product line. The M14K supersedes the M4K core, primarily for 32-bit microcontrollers. The M14Kc supersedes the 4KE core, offering an MMU for virtual-memory embedded operating systems.

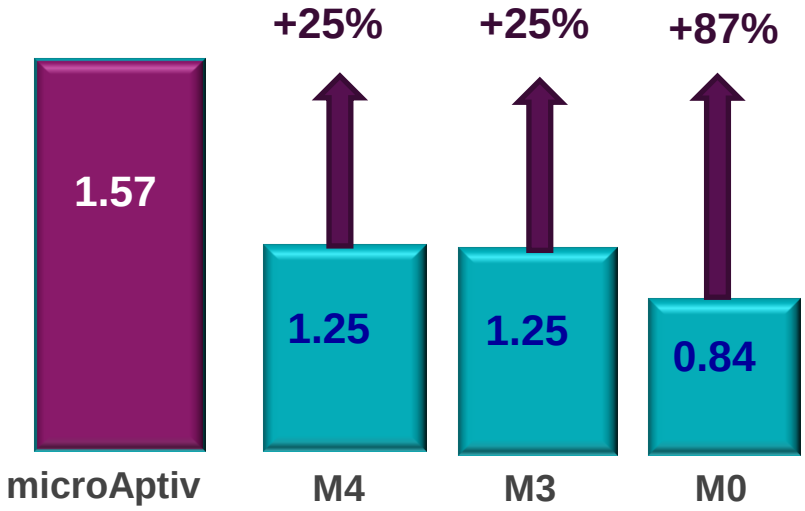
MIPS Fares Well Against ARM

Perhaps the most surprising result of comparing the new MIPS processors with ARM's best cores is that ARM no longer has a clear advantage in power consumption, core area, and performance. Usually, those are ARM's strengths.

For instance, using the data in Tables 2 and 3, we can compare the two microcontroller cores—the MIPS M14K and ARM Cortex-M3—in the same TSMC 90nm-G process. An area-optimized M14K will consume 11.6mW at 193MHz in 0.21mm^2 of silicon. A speed-optimized Cortex-M3 will consume 13.3mW at 191MHz in 0.37mm^2 of silicon. The M14K requires less power and silicon at virtually the same clock frequency. In power efficiency, the M14K wins, too: 25Dmips per milliwatt versus 17.9Dmips per milliwatt.

Note that we compared an area-optimized M14K with a speed-optimized Cortex-M3. That's because a speed-optimized M14K can reach a much higher clock frequency (295MHz). Assuming the two processors are clocked to deliver similar performance, the M14K will use less power and silicon. (The M14K has a throughput advantage of 1.5Dmips per megahertz versus 1.25Dmips per megahertz for the Cortex-M3.)

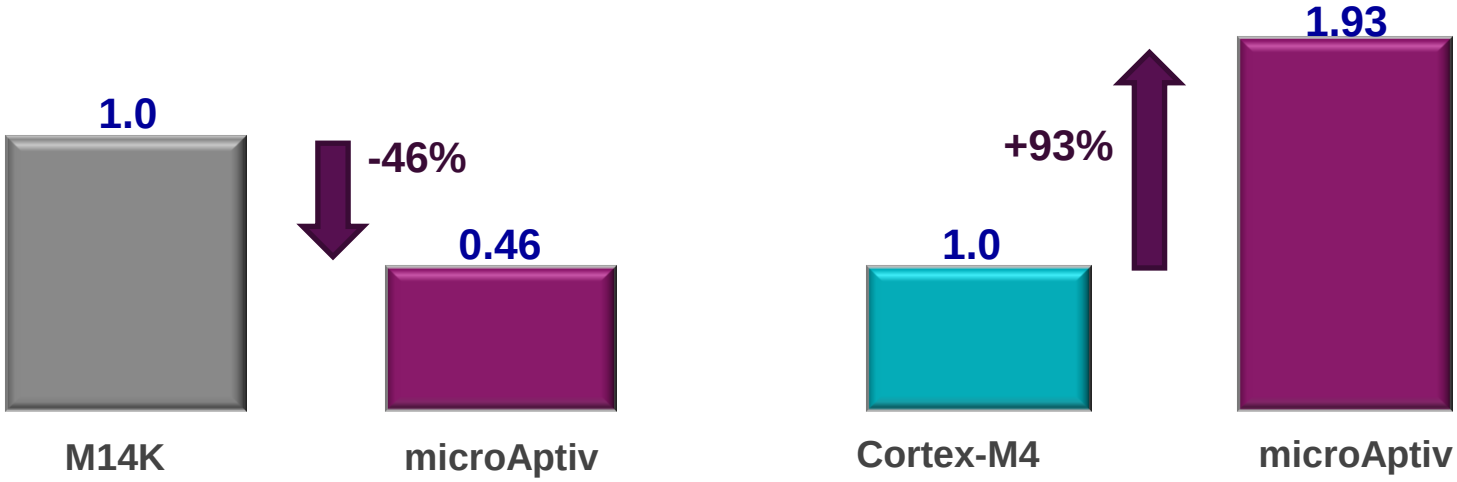
Better Performance vs ARM Cortex M Series



Dhrystone – DMIPS/MHz

- ❖ microAptiv outperforms Cortex M Series by up to 87%
- ❖ Lower clock speed needed to achieve equivalent performance

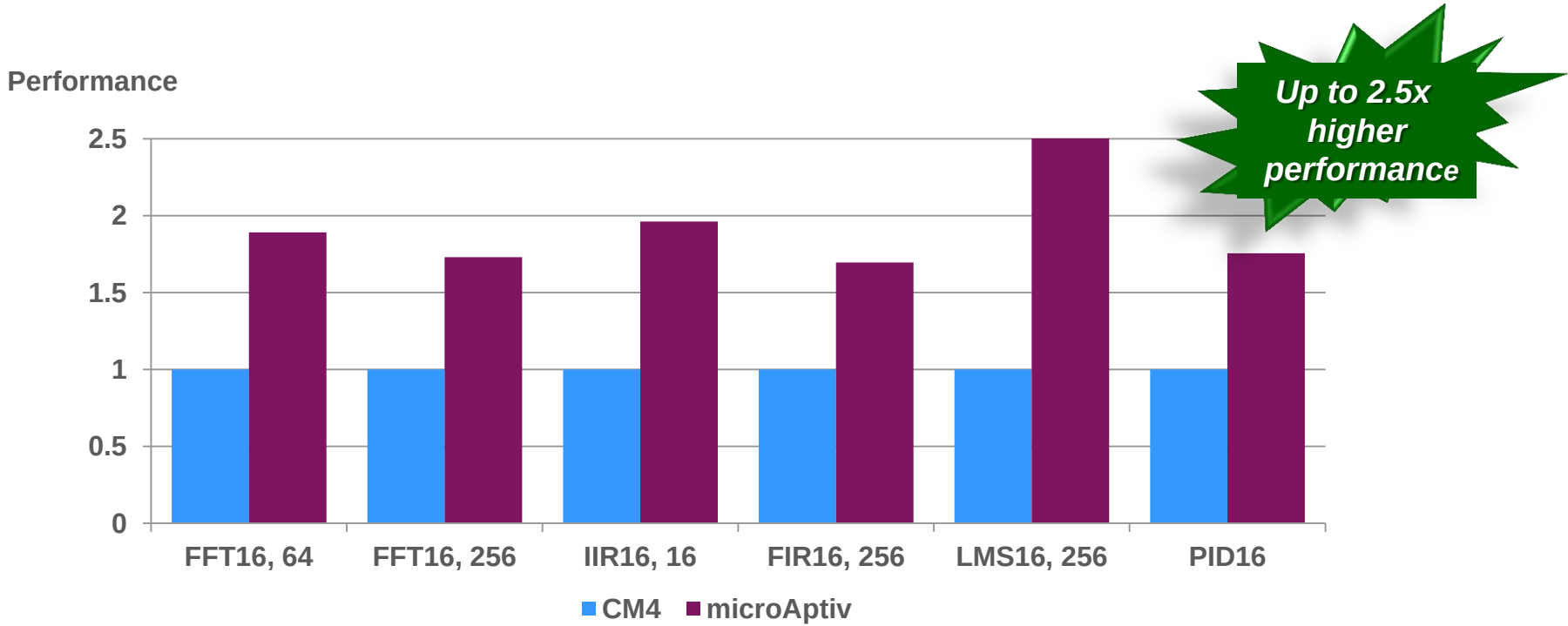
Better DSP Performance vs ARM Cortex M4



Running MIPS DSP Libs and ARM CMSIS DSP : FFT, FIR, IIR, LMS, PID, VMUL, H.264

microAptiv outperforms Cortex M4 by >90% for DSP operations

microAptiv vs. Cortex-M4 DSP Performance



Comparing DSP performance (higher is better) executing microAptiv DSP Library and Cortex M4 CMSIS Library

microAptiv vs Cortex-M Series Feature Comparison

Reduces Code Size With No Loss in Performance

Best Performance Efficiency

Better Real Time Performance

Faster Code Execution

More Flexible

FEATURE	microAptiv UC	Cortex-M3	Cortex-M0
Architecture	Harvard	Harvard	Von Neumann
Pipeline stages	5	3	3
ISA	MIPS32 and/or microMIPS	Thumb-2	Thumb/Thumb-2 (subset)
Legacy 32-bit decoder	Y - MIPS32 optional	N	N
Total instructions	300+	155	56
DMIPS Performance	1.57 DMIPS/MHz	1.25 DMIPS/MHz	0.9 DMIPS/MHz
Performance/Area Efficiency (90LP)	40 CM/MHz/mm2	27 CM/MHz/mm2	28 CM/MHz/mm2
GPRs	32	16	13
GPR sets (max)	16	1	1
Interrupt control	Y - int & ext	Y - int NVIC	32
Priority levels	8	4	4
Interrupt latency	10 cycles	12 cycles	16 cycles
Tailchaining	Y	Y	Y
MMU	Y - FMT	N	N
MPU (optional)	Y - up to 16 regions	Y - up to 8 regions	N
Multiply-Divide unit	Y	Y	Multiply only
Atomic bit instructions	Y	Y	N
Instruction-only trace	Y	N	N
PC sampling	Y	N	N
Perfomance counter	Y	N	N
Fast Debug Channel	Y	N	N
2-wire Debug	Y	Y	Y
Secure Debug	Y	N	N
Local Code Ram (max)	4GB	1GB	None
Local Data Ram (max)	4GB	1GB	None
Parity	Optional	N	N
Fast SRAM interface	Y	N	N
Flash memory prefetch	Y	N	N
External interface	AHB-Lite	AHB-Lite	AHB-Lite
Co-Processor interface	Y	N	N
Custom Instruction support	Y	N	N

microAptiv vs Cortex M4 Feature Comparison

FEATURE	microAptiv	Cortex M4
Core	M14K	Cortex-M3
Cache version	Y	N
Pipeline Stages	5	3
ISA	MIPS32 and/or microMIPS	Thumb2
Total instructions	300	155
DMIPS Performance (DMIPS/MHz)	1.57	1.25
Performance Efficiency (CM/mm2)	2200	2000
GPRs	32	16
GPR sets (max)	16	1
Closely coupled memory support	Y	N
MPU Support	Y	Y
MMU support	Y	N
Interrupt latency	10 cycles	12 cycles
Tailchaining	Y	Y
Instruction-only trace	Y	N
PC sampling	Y	N
Perfomance counter	Y	N
Fast Debug Channel	Y	N
Single wire debug	2-wire cJTAG	Y
FPU option	N	Y

microAptiv vs Cortex M4 Feature Comparison

DSP FEATURE	microAptiv	Cortex-M4
DSP Instructions	159	80
SIMD - 8/16	Y	Y
SIMD Instructions	70	38
Integer & Fractional data types	Y	Y
Saturate, Rounding options	Y	Y
Dedicated DSP/MDU unit	Y	N
Accumulators	Y (4)	N
Multiply/MAC instructions	38	29
32x32, 16x16, dual 16x16	Y	Y
16x8	Y	N
dual 8x8	Y	N
32x16	N	Y
Single cycle instructions	Y	Y
Shift Instructions	Y	N
Bit Manipulation	Y	Y
Compare/Pick	Y	N
Data Pack/Unpack	Y	Y
Bit Reversed Addressing	Y (instruction)	Y (instruction)
Modulo addressing	Y (instruction)	N

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Спасибо!