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MIPS 74K Goes Superscalar

New 32-Bit Processor Core Has Dual-Issue Out-of-Order Pipelining

By Tom R. Halfhill {5/29/07-01}

It's so old, it's new again. In the 1990s, MIPS Technologies was at the forefront of RISC microprocessor design, introducing speedy workstation/server processors like the R10000 with deep superscalar pipelines and out-of-order execution. Now those features are reappearing in synthesizable embedded-processor cores. At last week's **Microprocessor Forum** in San Jose, California, MIPS showed that architectural acrobatics are making a comeback. MIPS introduced the MIPS32 74K, a new family of 32-bit synthesizable processor cores for demanding embedded applications. Among other tricks, the 74K uses two-way superscalar superpipelining and out-of-order execution—techniques once dismissed as too complex for lowly embedded processors. MIPS estimates that a carefully designed and speed-optimized 74K can exceed 1.0GHz and deliver 1,800 Dhrystone mips when fabricated in a generic 65nm CMOS process.

This is a processor core with a 16- or 17-stage integer pipeline—the deepest such pipeline in any general-purpose embedded processor. The 74K has sophisticated dynamic branch prediction, improved DSP extensions, three privilege levels, an optional FPU, and a memory-management unit (MMU) with translation lookaside buffers to support virtual-memory operating systems. But the 74K isn't a retread of RISC designs from the 1990s. After three years of development, MIPS has devised an asymmetric superscalar pipeline that separates load/store instructions from other integer operations, with generous buffering between different sections of the pipes. These buffered pipelines—in concert with out-of-order execution—help minimize stalls and reduce the penalty for mispredicted branches.

What's missing from the 74K? Two cutting-edge features: hardware multithreading and provisions for coherent multicore integration. But those features may be coming. MIPS says a multithreaded version of the 74K is on the roadmap—indeed, the 74K's pipelines are designed with that feature in mind. A multithreaded 74K would be a logical progression from the MIPS32 34K family, which MIPS announced last year. The 34K is the first broadly licensed synthesizable processor core with hardware multithreading. (See *MPR 2/27/06-01*, "MIPS Threads the Needle.") Although the MIPS roadmap currently doesn't show a 74K-series processor with provisions for coherent multicore integration, the multicore trend is unstoppable, and the 74K will probably evolve in that way as well.

Essentially, the 74K is the MIPS response to ARM's Cortex-A8, the highest-performance ARM processor core and the first ARM processor with superscalar instruction issue. (See our two-part coverage in *MPR 10/25/05-02* and *MPR 11/14/05-01*, "Cortex-A8: High Speed, Low Power.") Although MIPS began developing the 74K long before ARM announced the Cortex-A8, both companies were thinking along similar lines. Both recognized the need for high-throughput processor cores in demanding embedded systems, such as high-definition audio/video products, broadband networking equipment, consumer-electronics devices with complex graphics, and any systems that depend heavily on Java software and powerful operating systems. MIPS has a strong presence in those markets.

It's no coincidence that both ARM and MIPS have turned to deep superscalar pipelines and powerful DSP

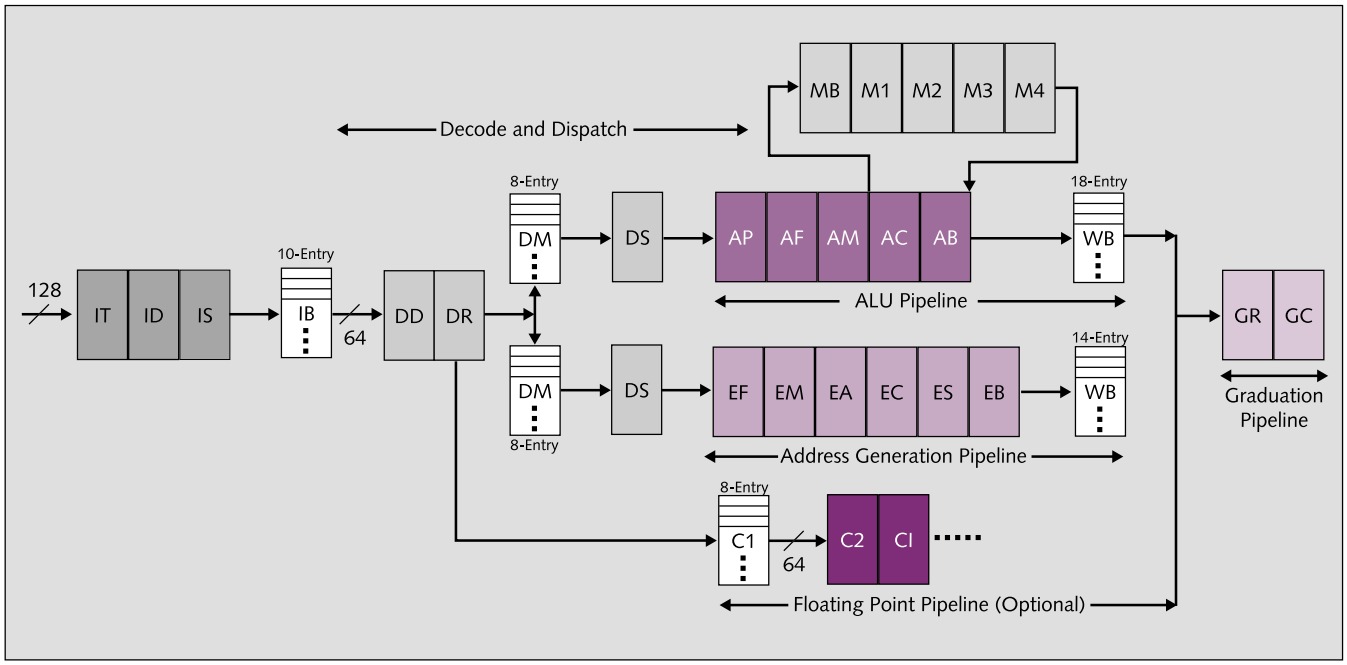

Figure 1. MIPS32 74K pipeline diagram. Note the numerous buffers, which prevent stalls, and the wide 128-bit interface to the instruction cache. The decode/dispatch unit decodes, renames, selects, and multiplexes the instructions for dual issue from a pair of eight-entry buffers. The ALU execution pipeline has six stages, beginning with AP, a no-operation stage that helps reduce the load/use penalty. Other stages handle bypasses and single- or multicycle instructions. The writeback stage is well buffered. The load/store execution pipeline has seven stages: EF (read register file and completion buffer), EM (bypass muxes), EA (compute addresses), EC (access cache), ES (another stage for accessing the cache), EB (a bypass stage), and WB (writeback, with buffering). The final two stages for all instructions are GR (graduation read) and GC (graduation commit), which retire the results of executed instructions from the writeback buffers.

extensions to reach the necessary level of performance. Although multicore SoCs based on lower-performance processor cores can meet some of those requirements, there's still interest in powerful single-core solutions that simplify hardware design and software development. Sometimes a single-core chip consumes less power, too.

Laying the Pipes

MIPS already has some powerful 32-bit embedded-processor cores. In addition to the multithreaded 34K, the MIPS stable includes the popular 24K and its sibling, the 24KE, which added DSP extensions in 2005. (See *MPR 5/31/05-01*, "The MIPS32 24KE Core Family.") Some MIPS customers integrate multiple 24K cores on a single chip or mate a 24K with a 24KE to get the horsepower they need. In some applications, a single 74K core can deliver performance equal to or better than those multicore designs. Single-core chips are easier to develop, and programmers don't have to partition their code among multiple processors. DSP extensions can eliminate the need for a separate DSP chip or core.

To obtain greater throughput from a single core, MIPS followed the usual two routes: higher clock frequency and improvements at the architectural and microarchitectural levels. Higher clock speeds generally require deeper pipelines to reduce the amount of execution logic in each pipe stage. The 74K's 16- or 17-stage integer pipeline is quite a bit deeper than the 34K's nine-stage pipeline and the 24K/24KE family's eight stages. By any standard for general-purpose processors, it qualifies as a superpipeline, exceeded only by much larger microprocessors for PCs and servers.

Doubling this superpipeline for two-way superscalar execution would have been a feat. However, simulations indicated that merely duplicating the pipeline wouldn't yield a worthwhile increase in the number of instructions executed per cycle. The deeper pipeline would run faster, but not more efficiently. Extensive analysis of instruction-pair combinations suggested the best way to partition the logic between the two pipelines. MIPS considered the balance of instructions executed in each pipe, the placement of the bypass points, and the relative positions of the ALU and address-generation stages. Using this modeling as a basis, MIPS decided to split the pipeline differently. The result is a 17-stage pipeline dedicated to load/store and branch instructions and a 16-stage pipeline for all other integer operations. (The optional FPU has yet another dual-issue pipe.) Figure 1 shows the 74K's pipeline.

Dividing the main pipelines in this manner reduces the amount of redundant logic. Each pipe has only the logic it needs to execute its own type of instructions. In contrast, a superscalar design with symmetric pipelines must duplicate all the logic. The 74K's asymmetric pipelines are faster, more economical, and power efficient—critical considerations for an embedded processor.

However, asymmetric pipelines are less versatile if the processor must execute instructions in order, because two instructions of the same type cannot execute in parallel. Additional modeling suggested that the asymmetric design would benefit from out-of-order execution. Also, the ability to execute instructions out of order could help hide the load/use penalty and ALU latency while reducing the number of clock cycles lost after mispredicting a branch.

Making Out-of-Order Trade-Offs

Superscalar pipelining is uncommon in 32-bit embedded-processor cores, but out-of-order execution is even more rare. It's guaranteed to raise eyebrows among the milliwatt misers. Out-of-order execution requires extra bookkeeping logic to keep track of instruction ordering, to retire completed instructions in their original program order, and to maintain a precise exception model. Among 32-bit synthesizable embedded-processor cores available for licensing, the only others with out-of-order execution are IBM's Power 440 and Power 460S. Both those processors are two-way superscalar machines, like the MIPS 74K, but they have much shorter seven-stage pipelines.

Undeterred by the challenge, the MIPS design team tailored an out-of-order mechanism especially for the 74K's asymmetric superpipelines. This mechanism relies heavily on buffers to decouple various sections of the pipelines from each other. It also minimizes the logic overhead by reducing the number of bypasses in the pipelines. Both pipes have all the penalty-free bypasses they need to reduce stalls, but they have fewer bypasses than a symmetric superscalar machine might have. Fewer bypasses minimize redundant logic and remove some limits on the processor's maximum clock speed.

Out-of-order execution allows the 74K's ALU to spread the execution of some integer instructions across multiple clock cycles. This aspect of the 74K will raise eyebrows among RISC diehards. To RISC designers of the 1990s (including the long-departed founders of MIPS), multicycle execution was a sin punishable by eternal damnation. However, the 74K's designers say that multicycle execution is well suited for this particular design. Unlike early RISC chips, the MIPS 74K is a synthesizable processor, which imposes some design constraints, especially when high clock frequencies are the goal. Indeed, some later RISC processors striving for high clock speeds also resorted to executing noncritical integer instructions in multiple cycles.

In the 74K, simple integer instructions still execute in one cycle, but others need two cycles, and a few require three cycles. (An example of a three-cycle operation is a multiply-accumulate [MAC] with saturation.) The combination of asymmetric pipelines and out-of-order execution allows the processor to hoist loads above other instructions, effectively hiding the latency of memory accesses. In addition, out-of-order execution helps the 74K run existing code more efficiently without recompilation. Although recompilation will improve performance, it's less important for an out-of-order processor than it is for a rigidly in-order machine. According to MIPS, good compatibility with existing binaries is a major concern for many customers.

One hazard the MIPS design team faced was the penalty for mispredicting a branch. Deeper pipelines typically levy greater misprediction penalties, because the processor must flush the partially completed instructions from the pipeline and refill it with new instructions from the branch-target address. In the 17-stage 74K, the penalty is a painful 13 clock cycles. (Note that the ARM Cortex-A8 suffers the same penalty, despite its shorter pipeline.) For this reason, the 74K has the best branch prediction of any MIPS processor.

While a program runs, three 256-entry branch-history tables and an eight-entry return-prediction stack keep tabs on frequently encountered branch instructions. Each table works independently, using a different method. These methods are based on the widely used G-share algorithm, assigning one of four possible scores to each branch (weakly taken, strongly taken, weakly not taken, strongly not taken). When the processor encounters a familiar branch instruction, all three tables vote on whether the program will take the branch again. The majority vote determines whether the processor will continue fetching from the current instruction stream or switch to the branch-target address.

Buffers and Wide Datapaths Prevent Stalls

Two important features of the 74K pipelines are their wide datapaths to the caches and their intermediate buffers. Both features prevent instructions from piling up in traffic jams that would stall the pipelines or fill them with bubbles.

The L1 instruction cache, like the L1 data cache, is a user-configurable option in the 74K processor. It can range in size to 64KB, is four-way set associative, has 32-byte cache lines, supports two outstanding cache misses, and has a 128-bit interface to the pipeline. This extra-wide datapath allows the processor to fetch up to four instructions per clock cycle—twice as many as it can execute per cycle. (Note that even if some instructions are 16-bit MIPS16e operations, the 74K still fetches a maximum of four instructions per cycle.)

Instructions flow from the cache into a ten-entry buffer, from which the decode/dispatch unit can issue two instructions per cycle to the superscalar sections of the pipeline. Integer instructions, still in program order, flow into a pair of eight-entry instruction buffers—one for the ALU pipeline and another for the load/store pipeline. These buffers act as windows onto the pending instructions. This is where the processor shuffles instructions out of order to maximize the number of dual issues. By this point, the processor has resolved enough dependencies to guarantee that all instructions issued to the ALU will not stall. Load instructions in the other pipeline may stall if their memory requests miss the data cache, but other instructions can bypass them, if there are no true data dependencies.

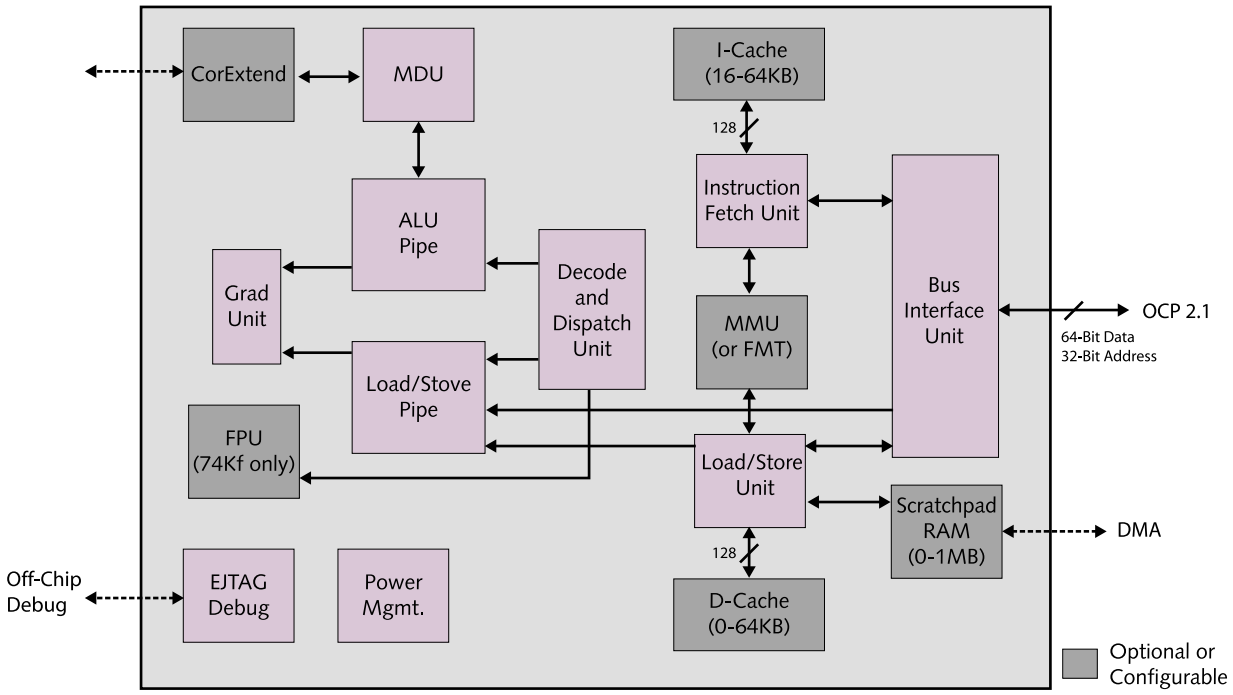

Figure 2. MIPS32 74K processor core block diagram. Note the optional or configurable features, which are typical of MIPS processors. CorExtend is standard, allowing developers to create their own application-specific extensions. The optional FPU connects to the CPU over an internal MIPS COP1 coprocessor interface. The external system interface is a 64-bit OCP 2.1 bus.

Additional buffers decouple the writeback stages of the pipelines from the execution stages. The ALU pipeline feeds into an 18-entry buffer, and the load/store pipeline feeds into a 14-entry buffer. These buffers prevent bottlenecks while the final two pipeline stages put the results of completed instructions back into program order and commit them to the registers or data cache. The optional L1 data cache can range in size up to 64KB, is four-way set associative, supports up to four nonblocking cache misses, and has a configurable 64- or 128-bit interface.

Counting all the pipeline buffers from start to finish, the 74K can hold 58 instructions in flight—not including the one- or two-dozen instructions moving through the pipe stages themselves. That's an impressively large window onto a running program, especially for an embedded processor.

Configurable Options Add Flexibility

Besides the caches, another user-configurable option is the FPU, which can perform single- or double-precision operations to IEEE 754 standards. In MIPS nomenclature, the integer-only version of the 74K core is the 74Kc, and the FPU version is the 74Kf.

If the FPU is present, the decode/dispatch unit can issue it two instructions per clock cycle—a load/store and an arithmetic instruction. At the same time, the decode/dispatch unit can issue two integer-type instructions. This capability allows the 74K to dispatch instructions at a peak rate of four instructions per clock cycle. However, floating-point loads and stores share the integer load/store pipeline, so the 74K cannot complete more than two instructions per cycle, even if the operations are a mix of integer and floating-point types. Furthermore, floating-point instructions always issue in order. Most execute at a throughput rate of one instruction per cycle.

The FPU connects to the CPU core over a MIPS-standard coprocessor interface (COP1). Note that this interface is dedicated to the FPU—the 74K lacks the external COP2 interface found on some MIPS processors. Instead, the only system interface is a 64-bit Open Core Protocol (OCP 2.1) bus with 32-bit memory addressing. Developers can use readily available gaskets to adapt this bus to AMBA-standard buses. (One such bridge is available for free download on the MIPS website.) Figure 2 is a block diagram of the 74K processor core, color coded to indicate which major blocks are optional or user configurable. At synthesis time, developers can configure many smaller features as well.

Both the 74Kc and 74Kf support the MIPS CorExtend technology for user-defined custom extensions. CorExtend gives MIPS developers some of the flexibility of user-configurable processor cores from ARC International and Tensilica. Developers can create custom instructions for specific applications, significantly boosting performance. Custom instructions can be single- or multicycle operations. CorExtend is optional in other MIPS processor families, but it's standard in the 74K family. (See *MPR 3/3/03-01*, "MIPS Embraces Configurable Technology.")

Another standard feature that's optional in some other MIPS processors is a high-performance multiply/divide unit (MDU) for integer operations. It's fully pipelined and five stages deep. It can execute 32- × 32-bit MAC instructions at a sustained rate of one operation per clock cycle. User-defined CorExtend instructions can use the 64-bit accumulators in the MDU for their own purposes.

New DSP Instructions for Video, VoIP, Speech

Depending on how the instructions are counted, MIPS has added about 44 new instructions to the DSP Application-Specific Extension (ASE). This DSP ASE Revision 2 is a standard feature of the MIPS 74K family. The DSP ASE first appeared in the MIPS 24KE in 2005 and is also found in the multithreaded 34K cores. (See the sidebar, "MIPS 24KE: Better Late Than Never," in *MPR 5/31/05-01*, "The MIPS32 24KE Core Family.") DSP ASE-R2 is a significant upgrade, expanding the number of instructions by about 50%. (The previous DSP ASE Revision 1 also added some instructions and three 64-bit accumulators to the package.)

According to preliminary tests by MIPS, the 74K can run some signal-processing code about 64% faster than the 24KE can. Thanks to deeper pipelines, the 74K can reach higher clock speeds, too, giving it an advantage of about 30% over the 24KE. Two-way superscalar execution can speed up critical inner loops by about 26%, according to MIPS. The chart in Figure 3 is based on preliminary internal benchmark testing under simulation.

Many new instructions in DSP ASE-R2 are the result of customer feedback. For example, one MIPS developer slashed the size of critical inner loops in a voice-over-IP (VoIP) application by about 50% by using only three new instructions (mulq_s.ph, mulq_s.w, and mulq_rs.w). Other new instructions perform element-wise vector arithmetic, dot-product operations, multiplications of fractional words, shift-and-insert operations, and byte-packing operations on 32-bit registers. Table 1 lists the new instructions in DSP ASE-R2.

DSP extensions for general-purpose processors have several advantages. Sometimes, a high-performance CPU/ DSP can outperform a dedicated DSP chip or core, as independent benchmarking by Berkeley Design Technology Inc. (BDTI) has shown. Hardware development and verification is much simpler with a single CPU/DSP core. Likewise, programmers

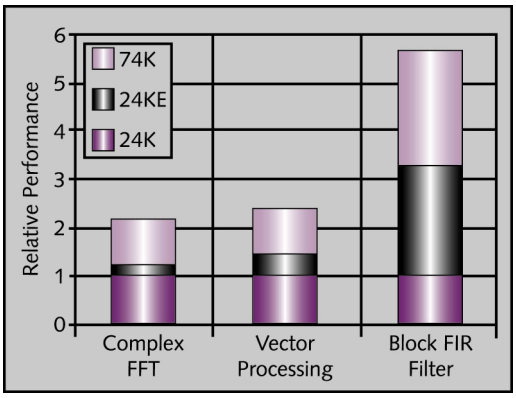

Figure 3. MIPS ran some internal DSP benchmark tests on cycle-accurate simulations of the 74K, 24KE, and 24K processors, obtaining these preliminary results. The 74K's performance is superior, thanks to a combination of higher clock frequency, dual-issue superscalar pipelining, and improved DSP extensions.

Instruction	Description	Comments	Instruction	Description	Comments
adduh.qb	Four-byte vector add, halve	Video	**shrav.qb**	Right-shift four bytes (register base)	—
adduh_r.qb	Four-byte vector add, halve, round	Video	**shrav_r.qb**	Right-shift four bytes, round (register base)	—
addu.ph	Halfword vector add	Video	**dpa.w.ph**	Dot-product accumulation	VoIP
addu_s.ph	Halfword vector add, saturate	Video	**dpax.w.ph**	Dot-product crossed operands, accum	VoIP
addqh.ph	Halfword vector add, halve	—	**dpaqx_s.w.ph**	Dot-product crossed operands, saturate, accum	VoIP
addqh_r.ph	Halfword vector add, halve, round	—	**dpaqx_sa.w.ph**	Dot-product crossed operands, saturate, accum	VoIP
addqh.w	Add two words, halve	—	**dps.w.ph**	Dot-product subtraction	VoIP
addqh_r.w	Add two words, halve, round	—	**dpsx.w.ph**	Dot-product crossed operands, subtraction	VoIP
subuh.qb	Subtract unsigned bytes, halve	Video	**dpsqx_s.w.ph**	Dot-product crossed operands, saturate, sub	VoIP
subuh_r.qb	Subtract unsigned bytes, halve, round	Video	**dpsqx_sa.w.ph**	Dot-product crossed operands, saturate, sub	VoIP
subu.ph	Halfword vector subtract	Video	**mul.ph**	Vector multiply halfwords	Speech
subu_s.ph	Halfword vector subtract, saturate	Video	**mul_s.ph**	Vector multiply halfwords, round	Speech
subqh.ph	Halfword vector subtract, halve	—	**mulq_s.ph**	Vector multiply Q15 halfwords, saturate	Speech
subqh_r.ph	Halfword vector subtract, halve, round	—	**mulq_s.w**	Multiply Q31 words to Q63 result, saturate	Speech
subqh.w	Subtract unsigned words, halve	—	**mulq_rs.w**	Multiply Q31 words to Q63 result, round	Speech
subqh_r.w	Subtract unsigned words, halve, round	—	**mulsa.w.ph**	Vector multiply halfwords, subtract, accum	Speech
absq_s.qb	Absolute-value four bytes, saturate	—	**cmpgdu.eq.qb**	Compare four bytes, equality	Video
precr.qb.ph	Reduce precision of four halfwords	—	**cmpgdu.lt.qb**	Compare four bytes, less than	Video
shrl.ph	Right-shift halfwords, insert zeroes	Video	**cmpgdule.qb**	Compare four bytes, less than/equality	Video
shrlv.ph	Right-shift halfwords, insert zeroes	Video	**append**	Shift-left word, insert bits from register	—
shra.qb	Right-shift four bytes	—	**prepend**	Shift-right word, insert bits from register	—
shra_r.qb	Right-shift four bytes, round	—	**balign**	Pack bytes from two registers into register	—

Table 1. New instructions in the MIPS DSP Application-Specific Extension (ASE) Revision 2. MIPS has expanded the DSP ASE by about 50%, making significant improvements over the original DSP ASE introduced in 2005. Note the additional instructions intended primarily for video, Internet telephony, and speech processing.

Characteristic	MIPS 74K
IC Process	TSMC 65nm GP
Standard Cells	TSMC
Memory Cells	Dolphin Technology
L1 Caches	32K I-cache 32K D-cache
Area (Core Only)	1.7mm^2
Area (Total)	2.5mm^2
Core Frequency (Worst Case)	>1.0GHz
Dhrystone 2.1	1.8 Dmips / MHz

Table 2. MIPS 74K performance characteristics after speed-optimized synthesis. MIPS has released this data for a 74K processor configured with 32K L1 caches and synthesized for maximum clock frequency in TSMC's 65nm GP (General Purpose) CMOS process. MIPS used TSMC's free standard cells. The processor's clock frequency exceeds 1.0GHz under worst-case conditions, not including on-chip variations and clock jitter.

can use a single tool chain to write and test their control code and signal-processing code, simplifying software development. The unified CPU/DSP instruction stream can make better use of on-chip memory and other resources, eliminating the need for redundant resources. And there's no need for separate CPU and DSP cores to exchange data over an on-chip bus that's slower than a CPU/DSP's internal datapaths.

Given all these advantages, it's no surprise that DSP extensions have become almost universal in general-purpose embedded processors. Although comparing DSP extensions across multiple architectures is beyond the scope of this article, the MIPS extensions are neither the best nor the worst of the lot.

DSP extensions for some competing architectures, such as ARM's Neon and Tensilica's Vectra DSP, offer more instructions and/or wider datapaths. But merely counting instructions is a superficial comparison; other factors are equally important. For instance, ARC's DSP extensions include configurable X/Y data memories with single-cycle access to multiple operands, as well as zero-overhead loops. Of course, additional features require additional silicon and power. The MIPS extensions strike a good balance for the target applications—mainly, consumer electronics and broadband communications. Customers can fill any gaps by using the MIPS CorExtend technology to define their own instructions for specific applications.

Different Paths to High Performance

With the 74K family, MIPS is pursuing a path to high performance long avoided by other vendors of licensable embedded-processor cores. Superpipelining, superscalar instruction issue, and out-of-order execution are widely considered too complex for synthesizable cores that must meet strict requirements for power efficiency.

Although ARM beat MIPS to the punch with the superscalar Cortex-A8, the ARM processor is a more conservative design, with its shorter, symmetric pipelines and in-order execution. Yet for ARM, the Cortex-A8 is a big stretch—the first superscalar processor from a company whose most popular product is the ARM7TDMI, a simple processor with a three-stage pipeline. ARM is climbing onto a limb with the Cortex-A8, because the processing demands of future cellphones are rapidly outgrowing the simple RISC cores that made ARM successful.

ARM says the Cortex-A8 can exceed 1.1GHz when fabricated in a 65nm CMOS process. To reach those heights, however, developers must use a partially hardened version of the core in combination with special high-speed Artisan synthesis libraries. (ARM acquired Artisan in 2004; see *MPR 9/7/04-01*, "ARM Extends Its Reach.") Last year, ARM announced a fully synthesizable soft-core version of the Cortex-A8 that has less headroom. So far, the fastest Cortex-A8 implementation is the Texas Instruments F1 core, which runs at a relatively conservative 550MHz in the OMAP3430 cellphone application processor. However, TI is manufacturing the OMAP3430 in a low-leakage 65nm CMOS process optimized for power efficiency, not for speed. TI says the F1 can surpass 1.0GHz if manufactured in a speed-optimized process. (See *MPR 7/24/06-01*, "The F1: TI's 65nm Cortex-A8.")

The MIPS 74K processor is a fully synthesizable soft core. MIPS says the 74K can exceed 1.0GHz under worst-case conditions when manufactured in a generic 65nm CMOS process—without prehardened elements like those in the Cortex-A8. Fully synthesizable soft cores are easier for developers to work with and are more portable to various synthesis libraries. Table 2 shows the 74K's characteristics when fabricated in the 65nm GP process from independent foundry TSMC.

Unfortunately, neither ARM nor MIPS has a track record of publishing certified EEMBC benchmark scores. It would be very interesting to see which company's approach to dual-issue superscalar pipelining is superior, especially under relevant workloads like EEMBC's digital entertainment suite. (See *MPR 2/22/05-01*, "EEMBC Expands Benchmarks.") Equally interesting would be the results with EEMBC's new power-measurement benchmarks. (See *MPR 7/17/06-02*, "EEMBC Energizes Benchmarking.")

MIPS has not yet released power-consumption estimates for the 74K, which makes any attempt to analyze the processor in context with the competition almost useless. (To be fair, apples-to-apples power numbers are almost impossible to obtain from any vendor.) MIPS does say that the 74K core requires about 800,000 to one million gates when synthesized for TSMC's standard-cell library and 65nm GP process. Of course, the gate-count is highly variable, depending not only on the processor's configuration but also on the synthesis parameters and cell library. MIPS says the core-area data in Table 2 is more useful for developers.

Looking Beyond ARM's Competition

ARM's Cortex-A8 is the rival to which the MIPS 74K will probably be compared most often, simply because ARM is

the market leader and the Cortex-A8 is also a superscalar design. However, MIPS faces competition with ARC, IBM, and Tensilica, too. MIPS prefers to exclude IBM from that list, saying that it rarely encounters customers that evaluate a licensable Power Architecture core against a MIPS core. That may be true today, but *MPR* expects the competitive landscape to change.

Although the Power Architecture is a latecomer to the processor-IP licensing market, it's an up-and-coming contender. Last fall, IBM announced its first new Power embedded-processor cores in seven years. (See the sidebar, "IBM's New Licensable Power Cores," in *MPR 11/27/06-01*, "Power.org's United Roadmap.") And last month, Freescale Semiconductor entered the licensing market with its Power e200 core. (See *MPR 4/2/07-01*, "Freescale Licenses Power Cores.")

Freescale's Power e200 isn't in the same league as the MIPS 74K, but IBM's processors are serious competition. IBM is now licensing five 32-bit embedded-processor cores, and four of them are two-way superscalar machines with out-of-order execution, like the MIPS 74K. Two of those IBM superscalar processors are soft cores: the eight-year-old Power 440 and the new Power 460S. Two are hard cores targeting IBM's 90nm CMOS process: the Power 464-H90 and the Power 464FP-H90, which has an FPU. The fastest of these processors can reach 1.0GHz at 90nm, and even the synthesizable Power 460S should be in that ballpark at 65nm, despite its relatively short pipeline.

The 32-bit processor cores licensed by ARC and Tensilica are entirely different animals. Compared with the MIPS 74K and IBM processors, the ARC and Tensilica cores are much simpler designs. They have relatively short five- or seven-stage uniscalar pipelines and in-order execution. ARC and Tensilica promise high performance through configurability and multicore integration. Their processors are

Feature	MIPS 74Kc	MIPS 74Kf	MIPS 34K	ARC ARC 750D	ARM Cortex-A8	IBM Power 460S	Tensilica Xtensa LX2
Architecture	MIPS32-R2	MIPS32-R2	MIPS32-R2	ARCompact	ARMv7	Power	Xtensa
Arch. Width	32 bits	32 bits	32 bits	32 bits	32 bits	32 bits	32 bits
Synthesizable	Yes	Yes	Yes	Yes	Yes*	Yes†	Yes
Pipeline Depth	17 stages	17 stages	9 stages	7 stages	13 stages	7 stages	5 or 7 stages
Pipeline Type	Out of order 2-way	Out of order 2-way	In order 1-way	In order 1-way	In order 2-way	Out of order 2-way	In order 1-way
Multithreading	—	—	1–5 threads	—	—	—	—
Branch Predict	Dynamic	Dynamic	Dynamic	Dynamic	Dynamic	Dynamic	—
L1 Cache	0–64K I/D	0–64K I/D	0–64K I/D	0–64K I/D	16–32K I/D	16–32K I/D	0–32K I/D (ECC)
L2 Cache	Optional	Optional	Optional	—	0K–1MB	—	—
L3 Cache	—	—	—	—	Optional	—	—
Scratchpad RAM	Optional Up to 1MB	Optional Up to 1MB	Optional Up to 1MB	Optional	Optional	Optional	Optional (ECC)
16-Bit Instr.	MIPS16e	MIPS16e	MIPS16e	ARCompact	Thumb-2	—	Yes
DSP Extensions	MIPS DSP ASE-2	MIPS DSP ASE-2	MIPS DSP ASE-1	Yes‡	Neon	Limited (MAC)	Optional Vectra LX
Java Extensions	—	—	—	—	Jazelle RCT	—	—
Custom Instr.	Yes	Yes	Optional	Yes	—	—	Yes
System Interface	OCP 2.1 64 bits	OCP 2.1 64 bits	OCP 2.1 64 bits	BVCI, AHB, AXI 32–64 bits	AMBA-3 AXI 64–128 bits	CoreConnect 64–128 bits	Xtensa PIF 32–64 bits
FPU	—	32/64 bits	Optional 32/64 bits	Optional 32 or 64 bits	Optional 32/64 bits	Optional 32/64 bits	Optional 32/64 bits
MMU + TLB	Optional	Optional	Optional	Yes	Yes	Yes	Optional
Privilege Levels	3	3	3	2	2 or 3	2	4
Debug Interface	EJTAG	EJTAG	EJTAG	JTAG	JTAG CoreSight	JTAG	JTAG
Max Core Freq (Process)	>1.0GHz 65nm GP	>1.0GHz 65nm GP	500MHz 90nm GP	700MHz 90nm GT	>1.1GHz 65nm	700MHz 90nm	440–475MHz 90nm G
Dhrystone 2.1	1.8 Dmips/MHz	1.8 Dmips/MHz		>1.5 Dmips/Mhz	2.0 Dmips/MHz	2.0 Dmips/MHz	1.6 Dmips/MHz
Power (Core)	n/a	n/a	0.56mW/MHz (90nm)	n/a	0.5mW/Hz 65nm	n/a	0.032–0.046mW/MHz 90nm G
Core Size (Process)	1.7mm² 65nm GP	n/a	2.1mm² 90nm GP	0.93mm² 90nm GT	<3.0mm² 65nm	n/a	~20k gates (base config)
Introduction	May-07	May-07	May-07	2004	2005	2006	2006

Table 3. Feature summary of synthesizable 32-bit embedded-processor cores targeting high performance. The MIPS 74K stands out as an aggressive design, sporting dual-issue superpipelines with out-of-order execution. IBM's Power 460S is also a two-way superscalar out-of-order processor, but it has much shorter pipelines. Nevertheless, it's capable of high clock speeds. ARM's Cortex-A8 is two-way superscalar, but it executes instructions in order and needs some prehardened elements to reach its maximum clock frequency. The ARC and Tensilica processors are simpler, more power-conscious designs that rely on custom extensions and multicore integration to deliver high throughput. Note that performance specifications will vary greatly, depending on processor configurations, synthesis parameters, cell libraries, the target fabrication process, and other factors. *The ARM Cortex-A8 is available as a fully synthesizable or a partially prehardened core. †IBM also offers versions of the 460S prehardened for its 90nm CMOS process, with or without FPU. ‡The base-configuration ARC 700 core includes DSP instructions, but the ARC 750D adds more. (n/a: data not available.)

Price and Availability

The MIPS32 74Kc and 74Kf 32-bit processor cores are available for licensing now. The 74Kc is the integer-only version, and the 74Kf has a 32/64-bit FPU. Both have the MIPS CorExtend technology, which allows customers to configure the cores and add their own extensions. MIPS doesn't publicly disclose license fees. For more information, visit:

- *www.mips.com/products/cores/32-bit_cores/MIPS32_74K_Family.php*

extensively customizable, and both companies specialize in processor-design tools that make it easier for customers to define application-specific instructions, registers, I/O buses, and other extensions. EEMBC benchmarks show that well-designed custom extensions can boost throughput to levels that would be impractical by merely increasing the clock rate. The catch is that someone must carefully profile the target application, create the custom extensions, and then write software to use the extensions.

MIPS Broadens Its Product Line

Table 3 summarizes the features of the 32-bit licensable embedded-processor cores with which the MIPS 74K is most likely to compete. To conserve space, the table lists only one such processor from IBM, the Power 460S. For specifications of IBM's other licensable cores, refer to the comparison table in *MPR 11/27/06-01*, "Power.org's United Roadmap." Likewise, the table lists only one processor each from ARC and Tensilica—their fastest cores that have optional DSP and FPU extensions.

Further comparative analysis must wait until MIPS releases more-detailed performance numbers and, especially, power-consumption estimates. Until then, *MPR* views the MIPS 74K as an impressive and aggressive design with uncertain power efficiency. The rising demands of high-definition video and broadband communications certainly create a need for higher performance. The challenge is to deliver that performance without busting the power budget.

With the previously announced 34K, MIPS introduced hardware multithreading. With the new 74K, MIPS is betting on superpipelining, superscalar issue, and out-of-order execution—as well as on multithreading, promised for a future member of the 74K family. PC and server processors reached the practical limits of all those techniques except multithreading a few years ago and are now resorting to multiple cores. Multicore SoCs are even more common in embedded systems. Yet powerful single-core SoCs remain attractive, too—until they reach the same limits that forced PC and server processors to incorporate multiple cores.

MIPS is offering customers many choices: low-power processors like the 4K family, midrange processors like the 24K/24KE, multithreaded processors like the 34K, and now the superscalar 74K. With CorExtend, some of these processors are highly configurable, too. No other company licenses such a broad line of processors and so many paths to higher performance. For SoC developers, this is truly the golden age.