MIPS-Classic Cores

Presented by Yuri Panchul
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MIPS Open Meetup in Moscow
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MIPS IP core product portfolio

1. Three classes of CPU Cores
2. I-Class brings the ultimate differentiation
3. Next 12-months focus on I-Class

P-Class

High single thread performance via OoO multi-issue design.
High data throughput apps

32-bit

P5600

MIPS32, multi-issue, 1-6 cores
VZ, 128b SIMD/FPU, 40b PA

P6600

MIPS64, multi-issue, 1-6 cores
VZ, 128b SIMD/FPU

I-Class

Performance/cost balanced
Efficiency via multi-threading
AP & RT embedded apps

64-bit

I6400

MIPS64, dual issue, 1-6 cores
SMT, VZ, SIMD/FPU

I6500

Many core/multi-cluster
Hetero cluster/multi-cluster
I6400 + DSPRAM, ITC, LL ports

I6500-F

FuSa version I6500
Safety Element out of Context (SEooC) design

32-bit

interAptiv

MIPS32, single issue, 1-4 cores
MT, DSP, FPU, MPU or MMU

I7200

nanoMIPS, dual issue, 1-4 cores
VMT, DSP, MPU/MMU, LL ports

M-Class

Size/Cost optimized CPUs
Class leading perf efficiency
IoT & embedded apps

32-bit

microAptiv

MIPS32/microMIPS,
MCU/MPU, SRAM/L1 cache
DSP, FPU (UCF), SRS

M5100/M5150

microAptiv +
VZ, FPU, Anti-Tamper

M6200/M6250

+30% higher frequency than microAptiv, M51xx
ECC, AXI, 40b PA, APB

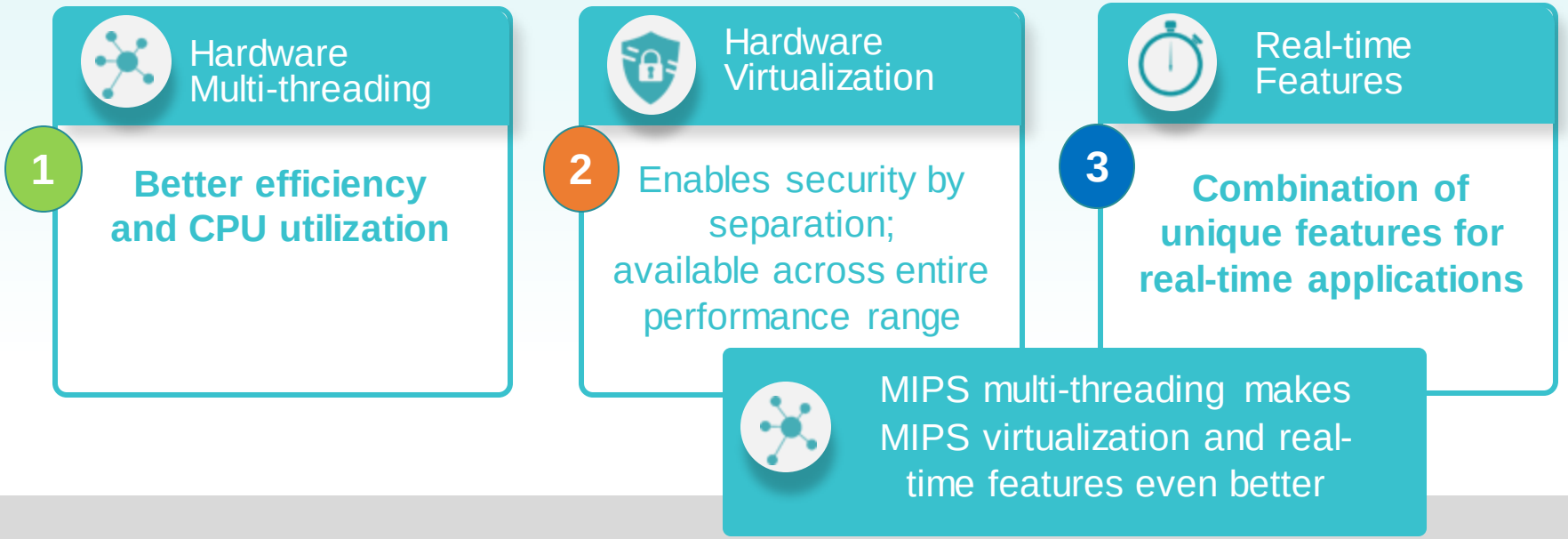
MIPS IP Cores - Features Summary

	microAptiv	*M51xx*	M62xx	interAptiv	*I7200*	*I6500/-F*	*P5600*	*P6600*
MIPS Primary ISA	MIPS32 r5	MIPS32 r5	MIPS32 r6	MIPS32 r5	nanoMIPS32	MIPS64 r6	MIPS32 r5	MIPS64 r6
Virtual/Phys Addr Bits	32/32	32/32	32/32	32/32	32/32	48/48	32/40	48/40
FPU	✓ (UC version only)	✓	-	MT	-	MT w/SIMD	Hi Perf w/SIMD	Hi Perf w/SIMD
DSP/SIMD extensions	DSP ASE r2	DSP ASE r2	DSP ASE r2	DSP ASE r2	DSP ASE r2	MSA 128-bit	MSA 128-bit	MSA 128-bit
Virtualization	-	✓	-	-	-	✓	✓	✓
Small code size ISA	microMIPS32	microMIPS32	microMIPS32	MIPS16e2 ASE	nanoMIPS32	-	-	-
Multi-threading	-	-	-	2 VPE, 9 TC	3 VPE, 9 TC	4 VPE	-	-
SuperScalar	-	-	-	-	Dual-issue in order	Dual-issue in order	Multi-issue OoO	Multi-issue OoO
Pipeline stages	5	5	6	9	9	9	16	16
Relative Frequency*	0.6x	0.6x	0.75x	1x	0.95x	0.90x	1.10x	1.10x
SPRAMs (I/D/U)	✓ / ✓ / -	✓ / ✓ / -	✓ / ✓ / -	✓ / ✓ / -	✓ / ✓ / ✓	- / ✓ / -	- / - / -	- / - / -
L1 caches	✓	✓	✓	✓	✓	✓	✓	✓
L2 cache	-	-		✓	✓	✓	✓	✓
Coherent Multi-Core	-	-	-	Up to 4 cores	Up to 4 cores	Up to 6 cores, Up to 64 clusters	Up to 6 cores	Up to 6 cores
Native System Bus I/F	AHB-Lite	AHB-Lite	AXI	OCP 2 or AXI	AXI	AXI or ACE	AXI	AXI

* Relative Frequencies are approximate, are provided for rough guidance only, and will vary to some extent in different process nodes

MIPS technology differentiation

MIPS architecture and IP cores offer powerful, unique capabilities



MIPS IP cores

1. Offer leading Power Performance Area (PPA) across the range
2. Provide ultimate scalability: multi-thread, multi-core, multi-cluster
3. Address Functional Safety to ISO 26262 for automotive and IEC 61508 for industrial

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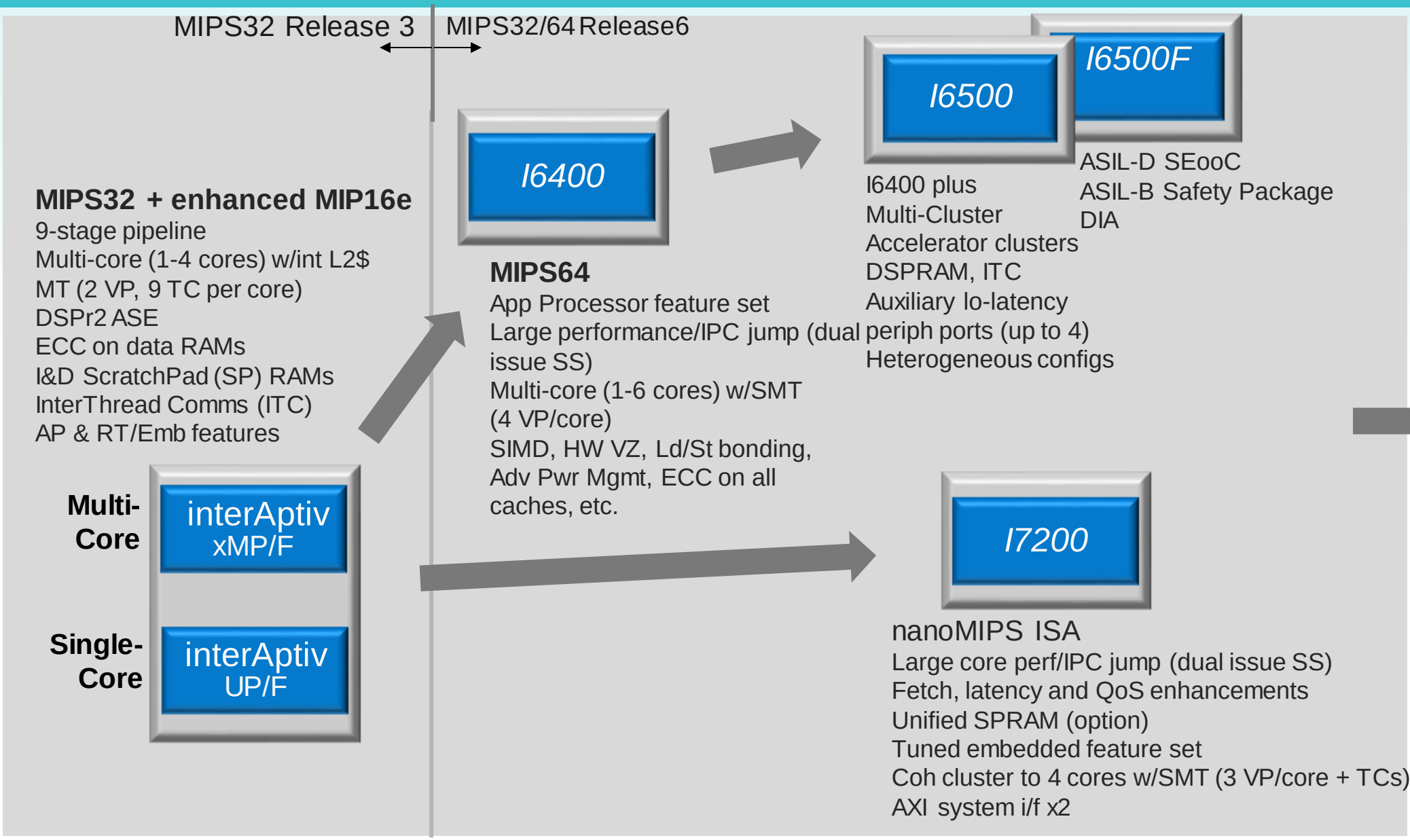
The I-Class

I6500

I7200

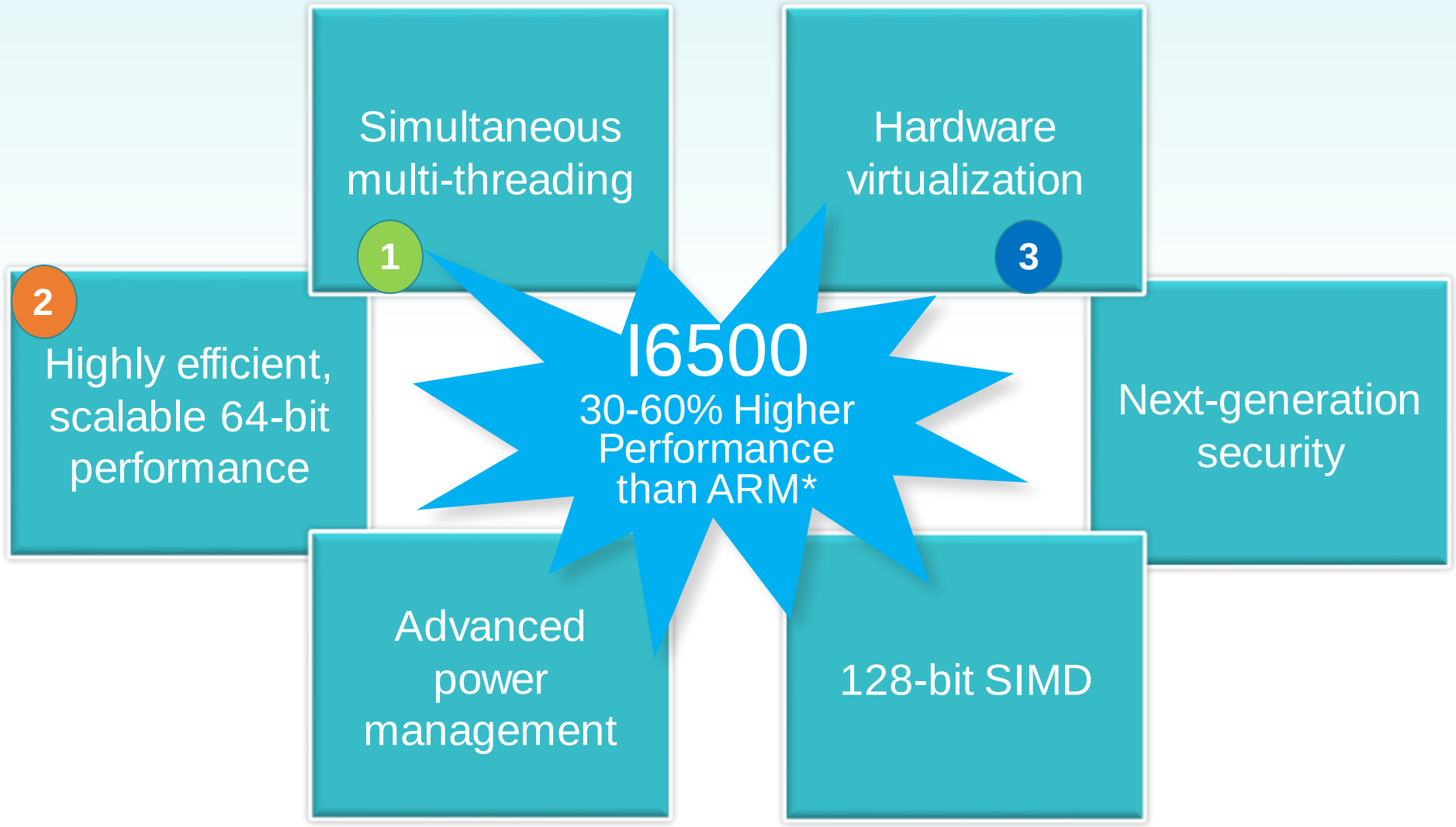
MIPS® I-Class Processor Core Roadmap

MIPS32 and MIPS64 evolution



Highly efficient, scalable MIPS Warrior I6400 & I6500

Setting a new standards in mainstream 64-bit processing



Key Components of a Multi-Core Cluster?

I6500

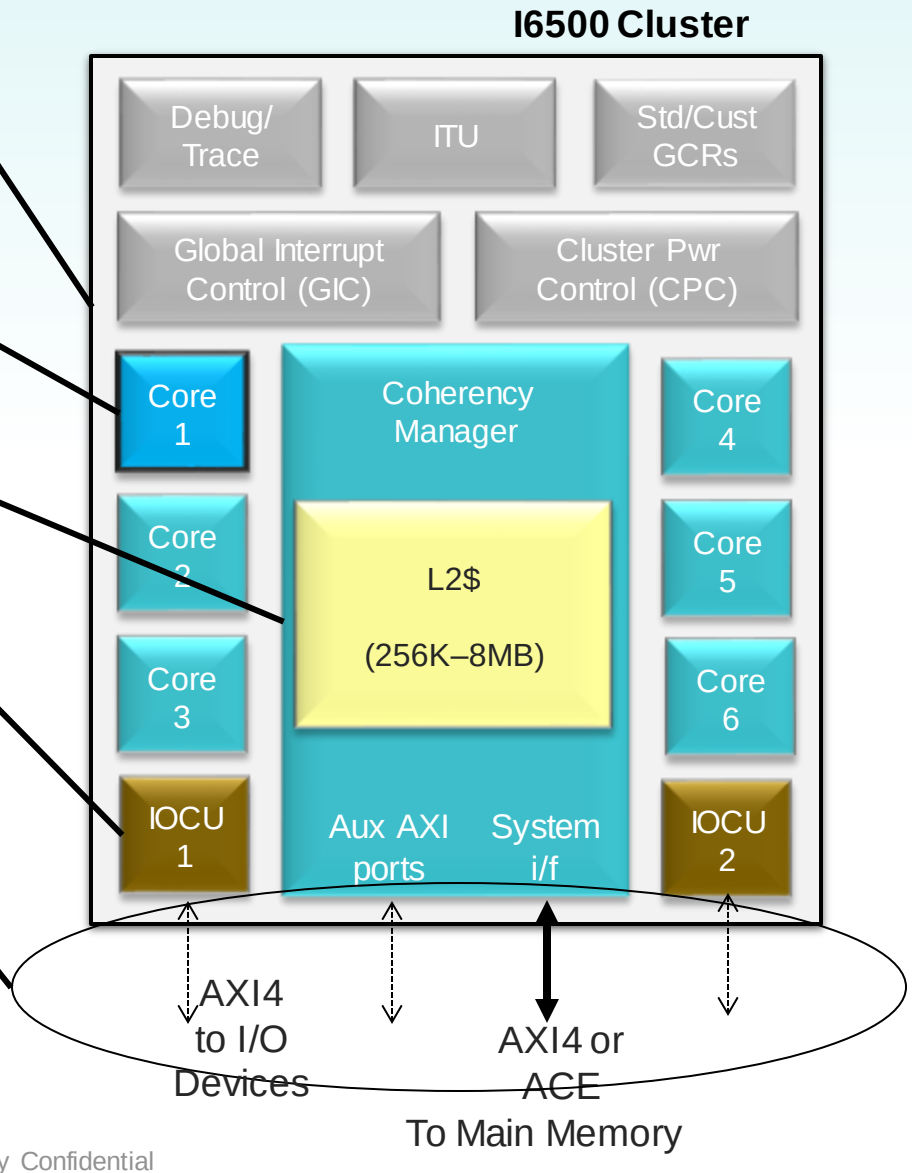
CPU Cluster : contains multiple CPU Cores, Coherent IO Cores and other supporting CPU Subsystem

MIPS CPU Core: 1 to 4/6 cores / Cluster

Coherency Manager : handles CPU – CPU – IOCU memory transactions coherently

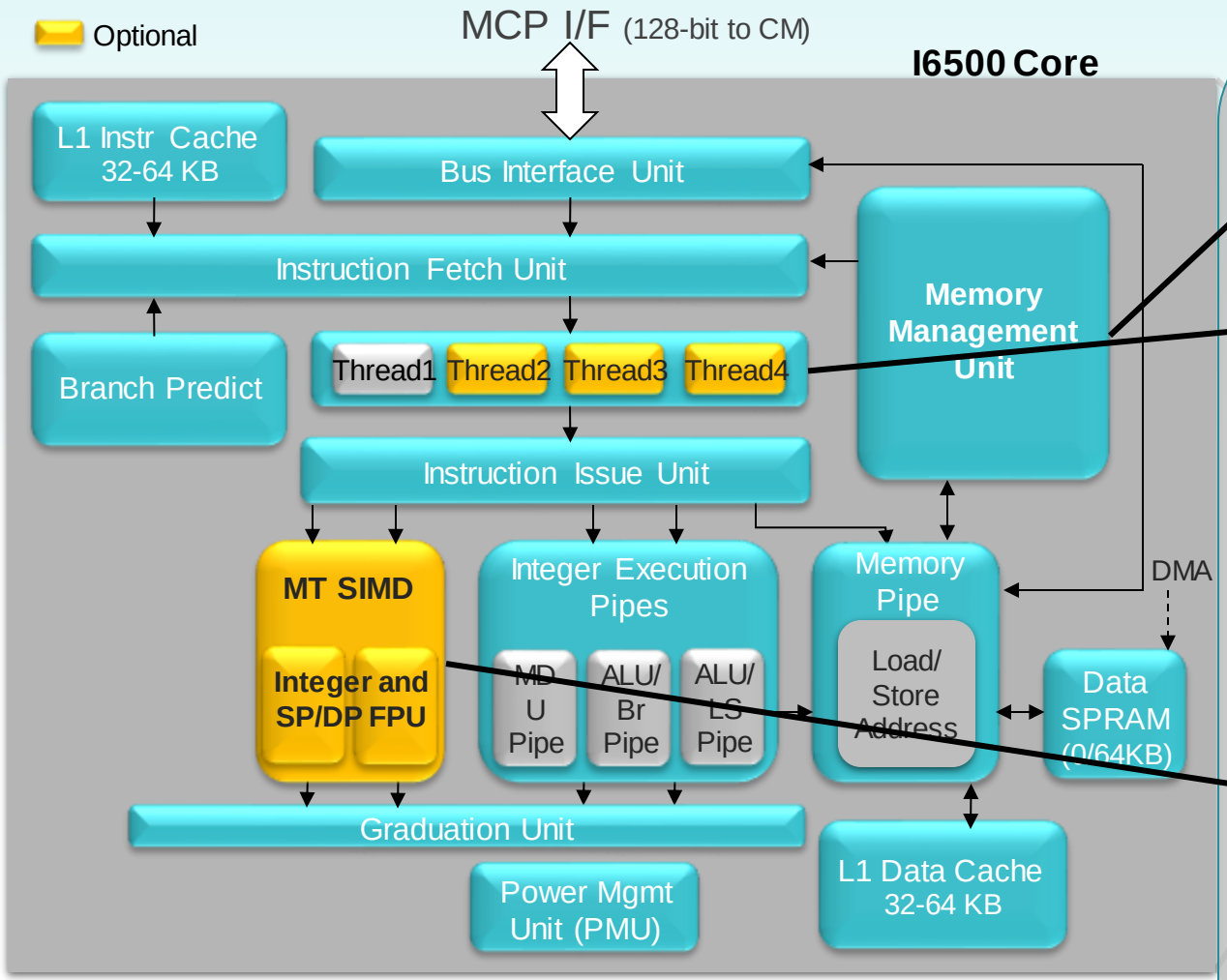
IOCU: 2-8 Coherent IO interface for fast CPU interface to system IO

Cluster Interface: Combination of Industry standard interfaces.
ACE – **A**XI4 **C**oherency **E**xtension



How to build a Multi-Core Cluster?

I6500



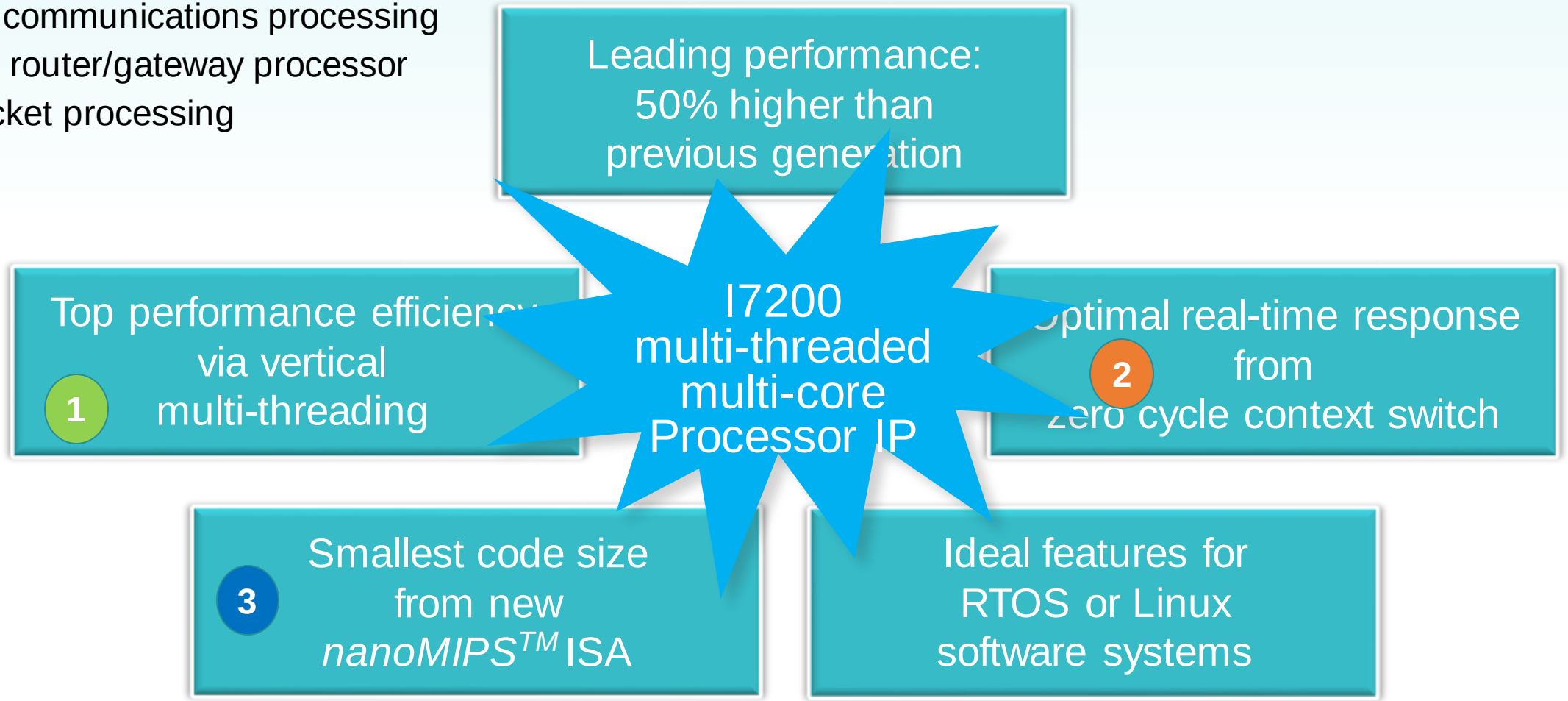
MMU : enable OS like Linux to manage memory efficiently as well as enforcing memory isolation and protection.

SMT (Multi-Threading): up to 4 hardware threads makes I6500 behave like 4-CPUs. Each hardware thread adds ~10% area; 1st thread, boost throughput by as much as 50%

SIMD (Single Instruction Multiple Data): Vector level Arithmetic and Boolean engine working. Ability to execute multiple math operation per cycle.

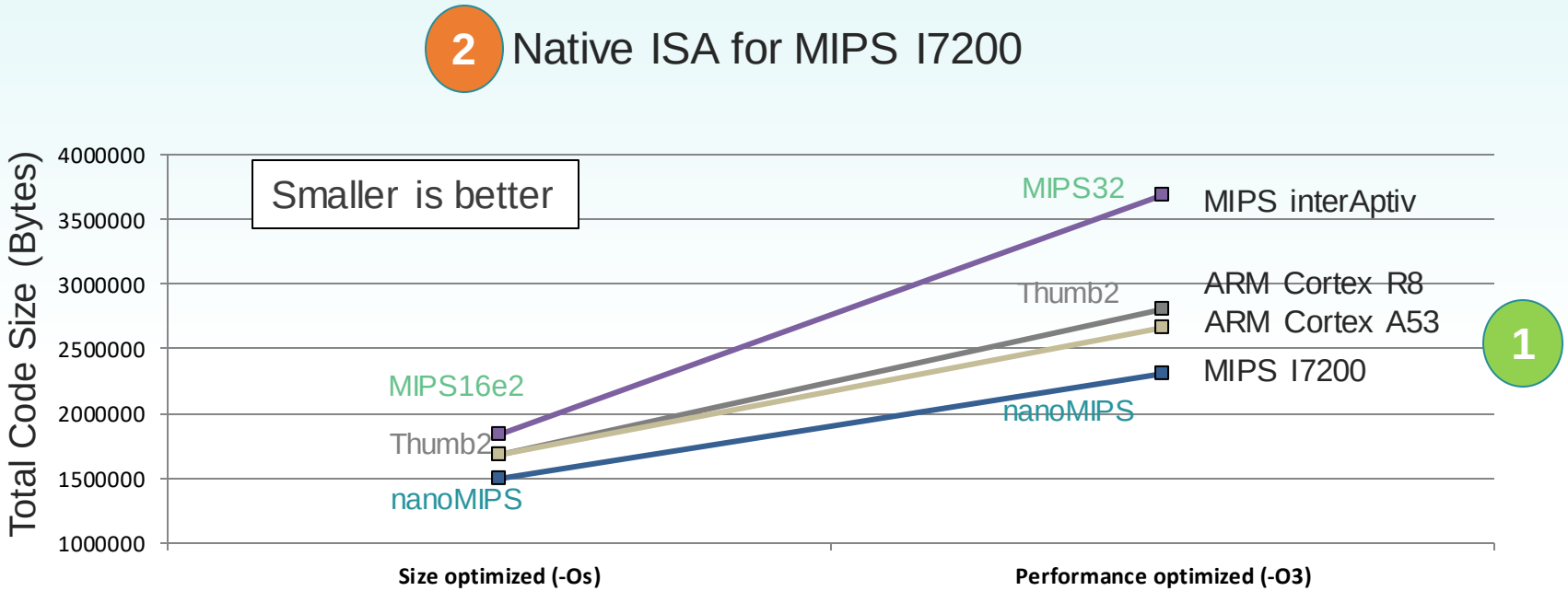
MIPS I7200 Highlights

- **Multi-threaded multi-core 32-bit processor IP**
- **Designed for high performance embedded systems with real-time requirements**
  - LTE/5G, communications processing
  - Wireless router/gateway processor
  - Data/packet processing



nanoMIPS ISA – advancing small code size

3 Achieves outstanding code density targeting small footprint applications or constraint devices



gcc compiler, with indicated optimization target

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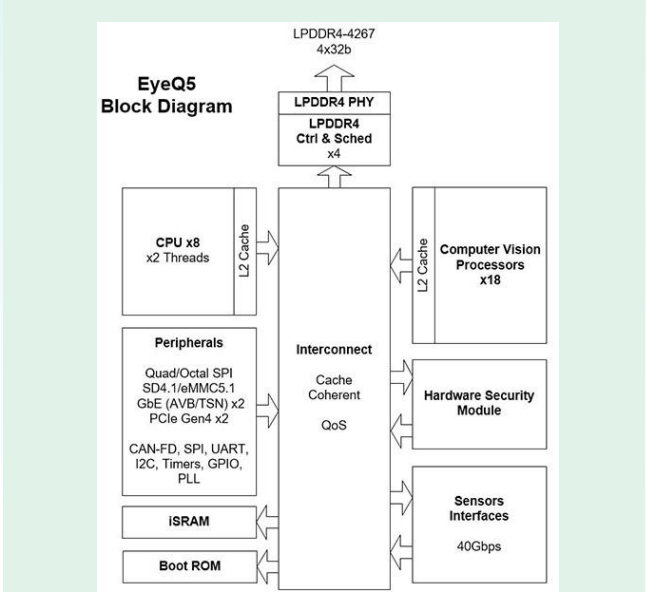
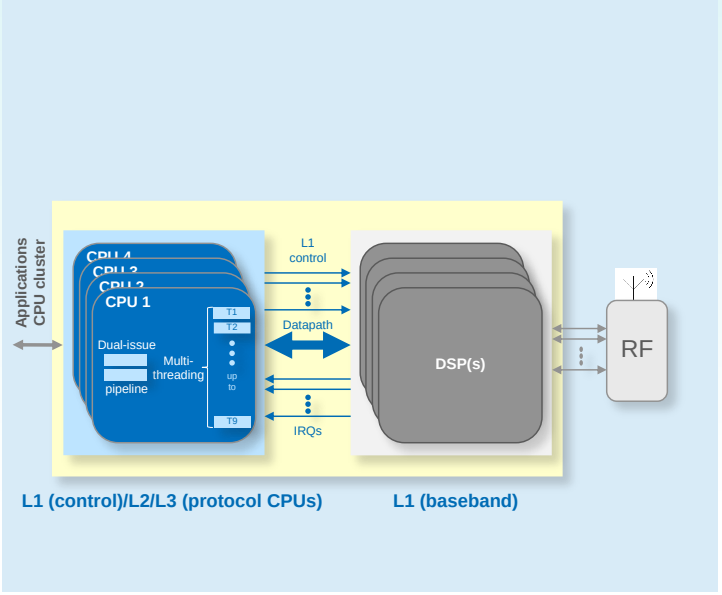
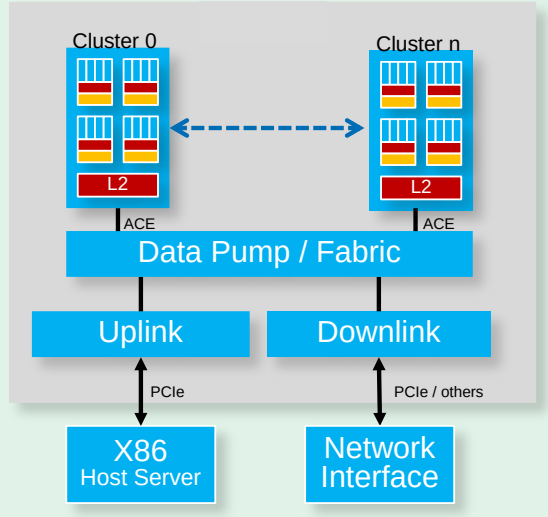
Success Stories

Market specific use-cases

Classical Application Segments







Feature	ADAS	LTE/5G	Datacenter
Application 1	Autonomous driving	Broadband LET modem	Converged Infrastructure. Distributed Workload processing
Value Prop 2	SMT, RT, IPC, VZ	SMT, RT, IPC, low power, small code	SMT, RT, IPC, distributed work load, VZ
Key drivers 3	Heterogeneous, FuSa / SEooC, multi-Cluster	High efficiency class leading 32b uArch High perf small code size ISA Low latency embedded / RT features	Threads / cores / clusters low latency payload processing
Likely Customers	Denso, Renesas, NXP, OnSemi, Samsung, Toshiba, Cypress, STM, Microchip, Bosch,.. Baidu, Argo, …	MTK, UniSoc, Qualcomm, Sony,	Cisco, Huawei, Broadcom, Marvell, Juniper, Google,

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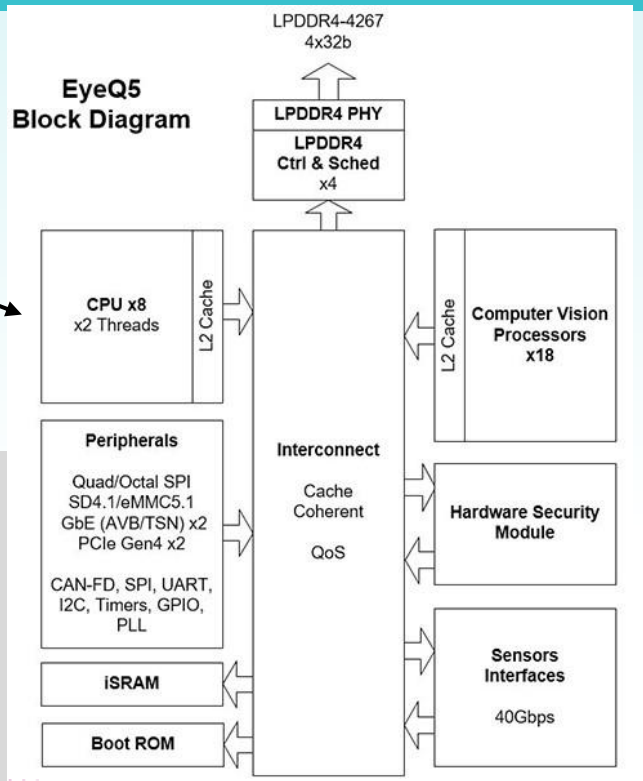
Application Segment 1
ADAS

I6500-F lead customer: Mobileye ADAS Platform

I6500-F at heart of heterogeneous coherent processing clusters in next-gen EyeQ®5 SoC

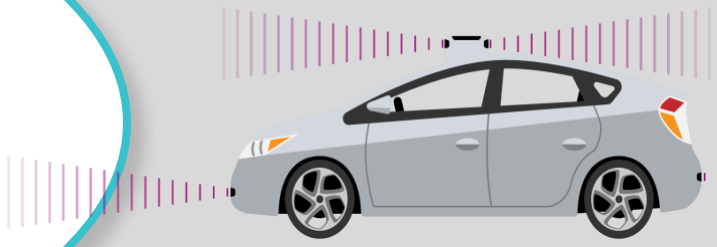
Designed to act as central computer for sensor fusion in Fully Autonomous Driving (FAD) vehicles starting 2020



"Our EyeQ®5 SoC will be the most advanced solution of its kind for fully autonomous vehicles which will start rolling out in 2020. The ASIL B(D) features in the I6500-F are key to ensuring our chip achieves the highest level of safety."

2018

– **Elchanan Rushinek, SVP Engineering, Mobileye**



MOBILEYE
An Intel Company

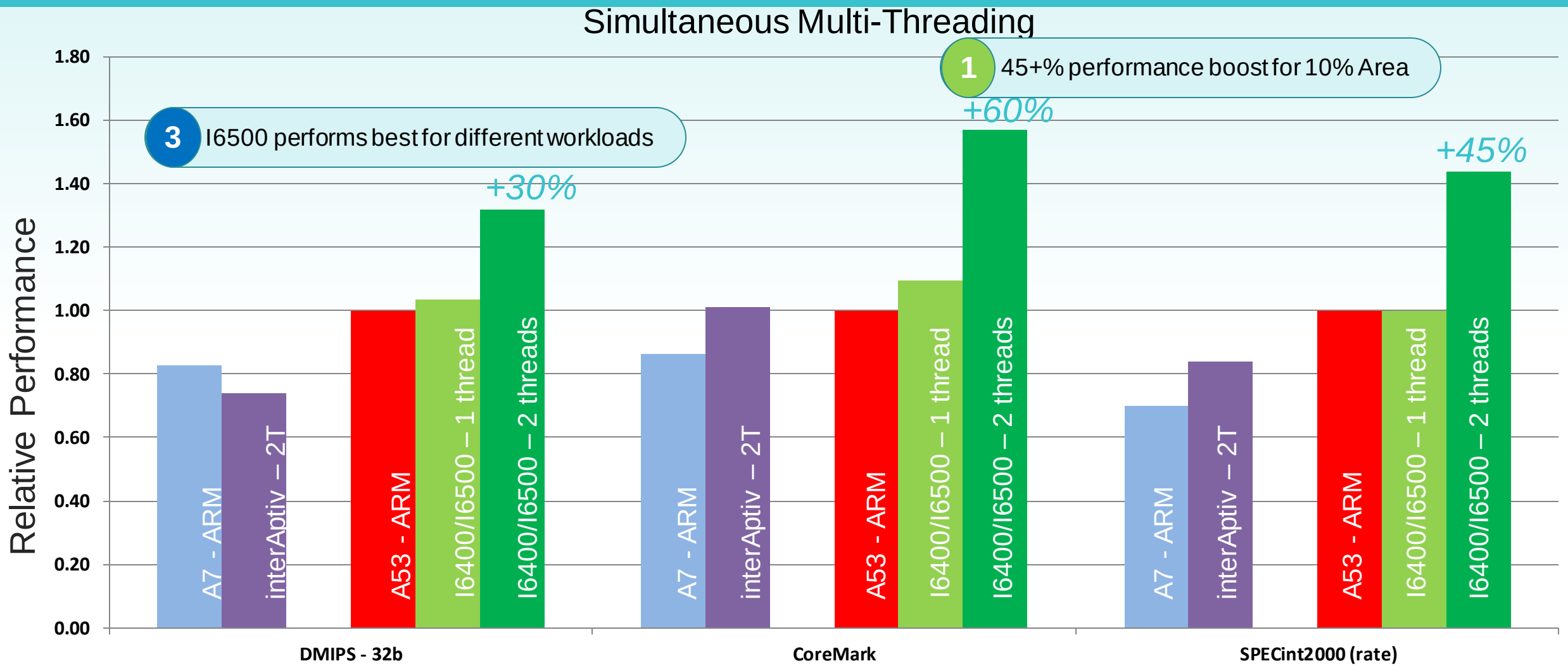
MIPS I-class vs Cortex A7 & A53 performance

Per core, normalized to A53 Values (@ same frequency)

2 Less power or more CPU headroom

1 45+% performance boost for 10% Area

3 I6500 performs best for different workloads



- Based on Cortex A53 data reported by ARM on website and/or in presentation materials, plus benchmarked results on Linaro (HiSilicon Octa A53 Kirin620) with Linux kernel: 3.18.0-linaro-hikey SMP preempt, RFS Debian squeeze, with GCC-based 5.0.0 toolchain. A7 scores are ARM claims. Measured results are lower.
- I6400 results are based on production released RTL, FPGA platform benchmarking and in case of SPEC, 1 enhancement for next release performance models testing

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Application Segment 2
LTE/5G

Success Story, Multi-threading & Mediatek

I7200

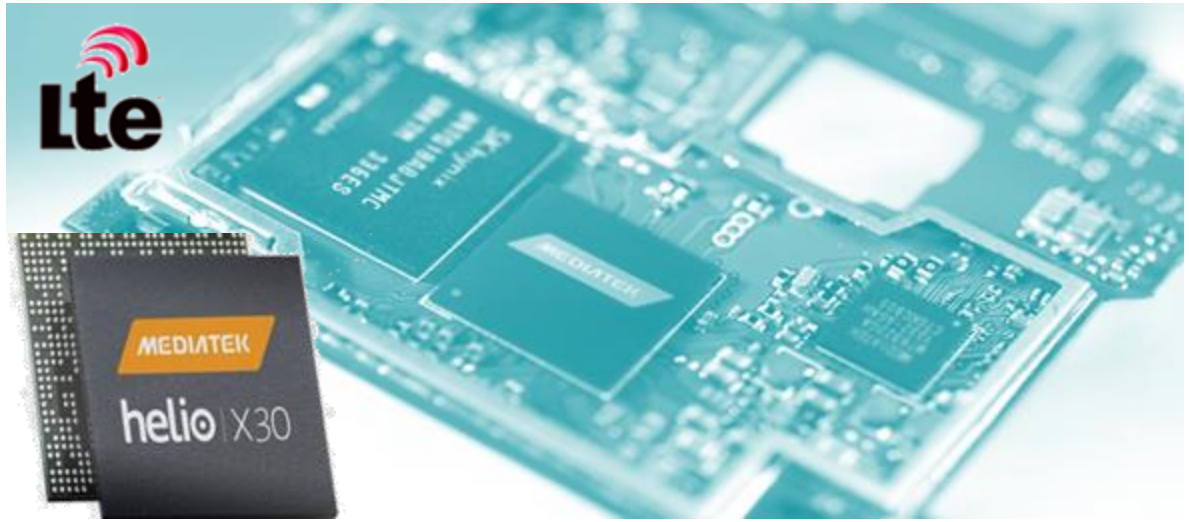
Mediatek 5G LTE modem

LTE

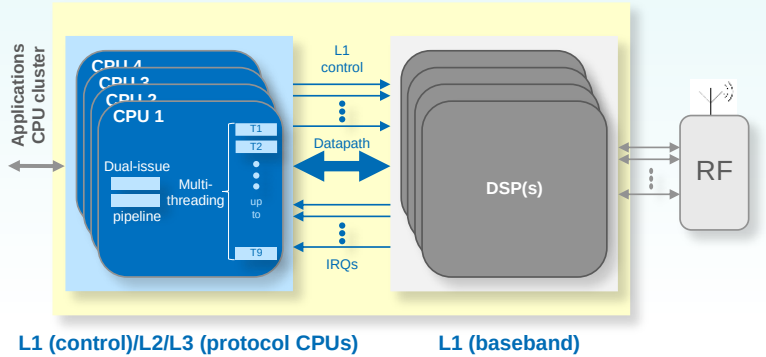
- Mediatek designed MIPS into modem across multiple products
- First version, Helio X30, in production

MIPS Advantage

- **Hardware Multi-Threading (MT)**
  - Fast inter-thread communications
  - Higher performance/high processing efficiency
- **Scalability**
  - 1-4 cores, 2 threads per core
- **Deterministic ; Real-time interrupts**

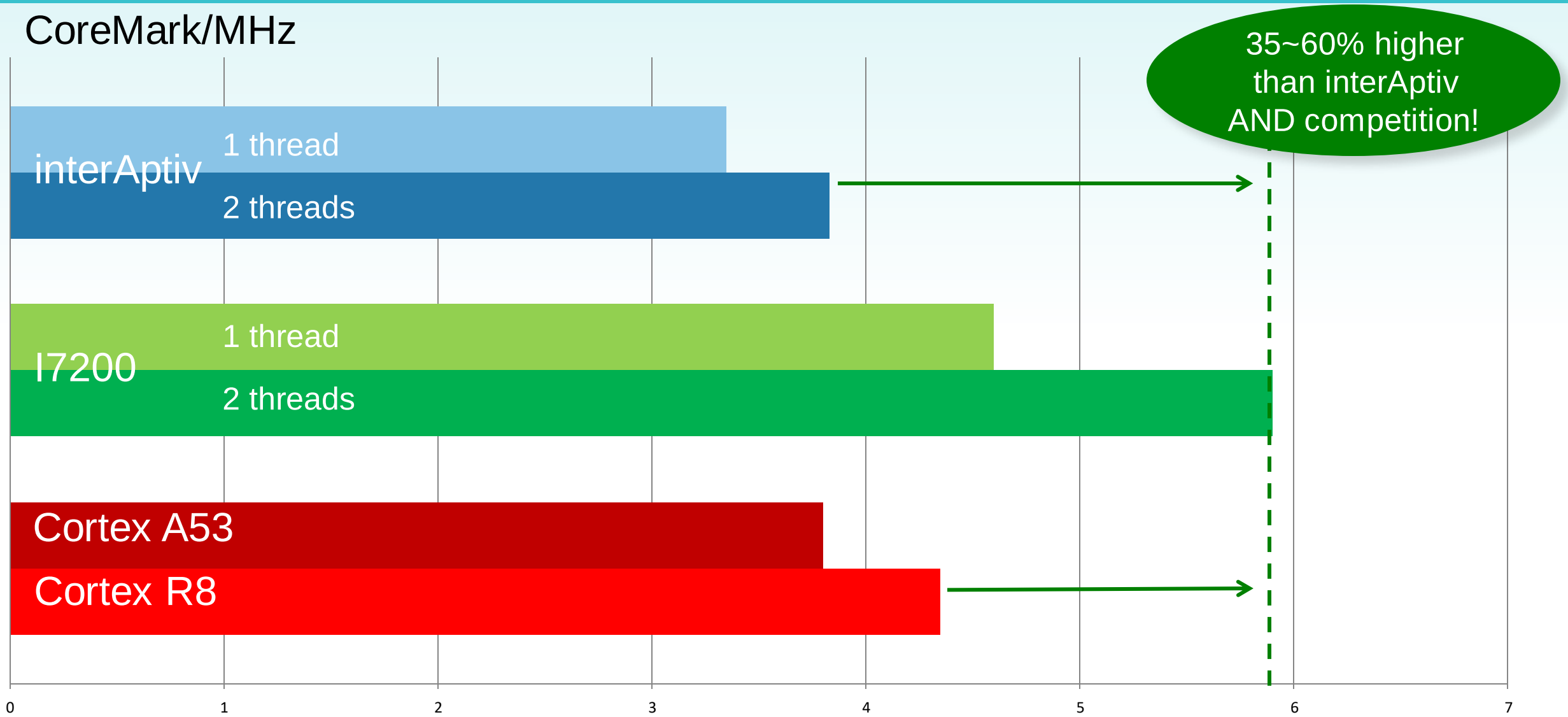


About MIPS in the application



"MIPS CPUs, with their powerful multi-threading capability, offer a combination of efficiency and high throughput for LTE modems that contributes significantly to system performance." ***said Dr. Kevin Jou, SVP and CTO, MediaTek***. **2018**

I7200 Performance Advantage



ARM scores reported by ARM for AArch32. Thumb2 scores likely 5-10% lower.
MIPS scores are MIPS32 for interAptiv, and nanoMIPS for I7200

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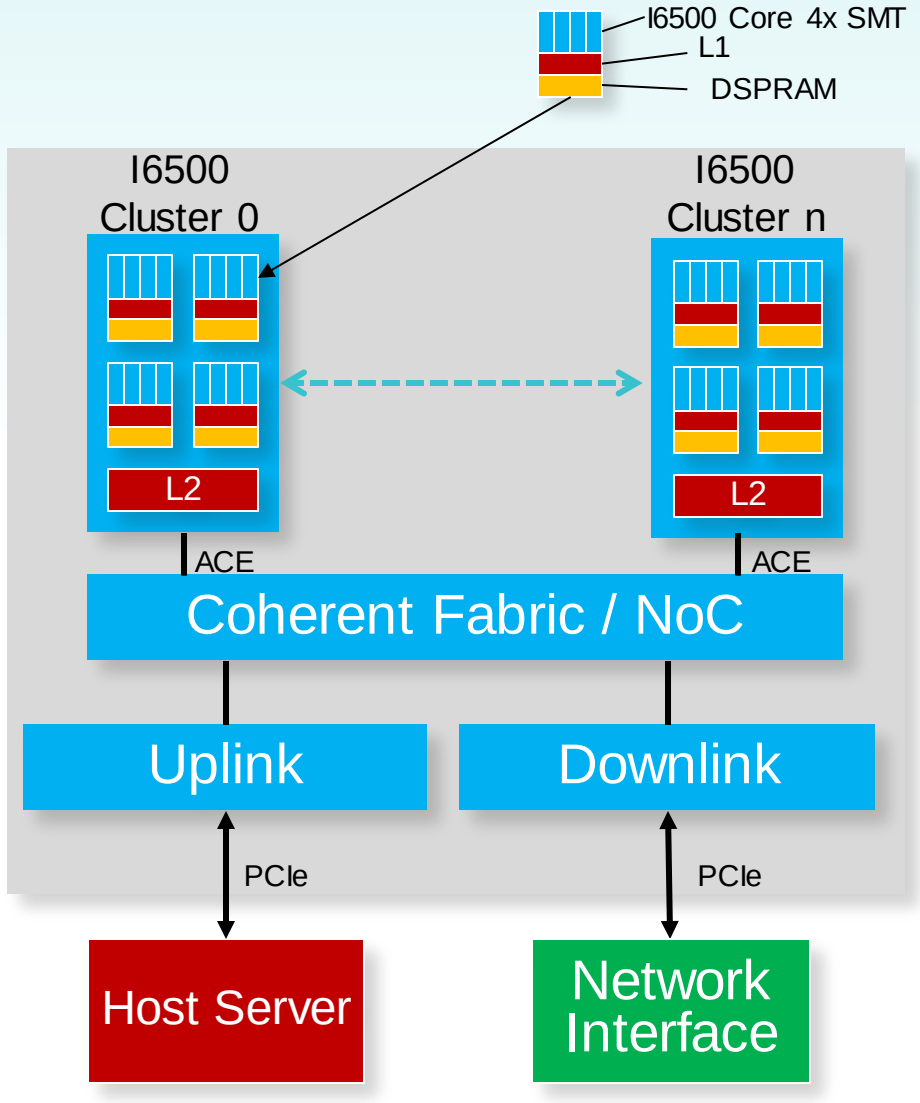
Application Segment 3
Data-center

Datacenter

Distributed Workload Processor

1. **Scalable - Multi-threading to Multi-core to Multi-cluster**
   - **Configurable - Heterogeneous inside & outside**
2. **Optimized for High-throughput data processing applications**
3. **Real-time, secure, deterministic and low latency**



"The MIPS Simultaneous Multi-Threading architecture is an important technique to ensure that such workloads run efficiently as measured by the CPU's instructions per clock, or IPC. We have seen that this efficiency translates directly into a smaller area as well as lower power for silicon implementations based on MIPS." 2018

Pradeep Sindhu, CEO of Fungible

I6400 & 6500 – Why Multi Threading?

A powerful differentiator among CPU IP cores

1 Why MT?

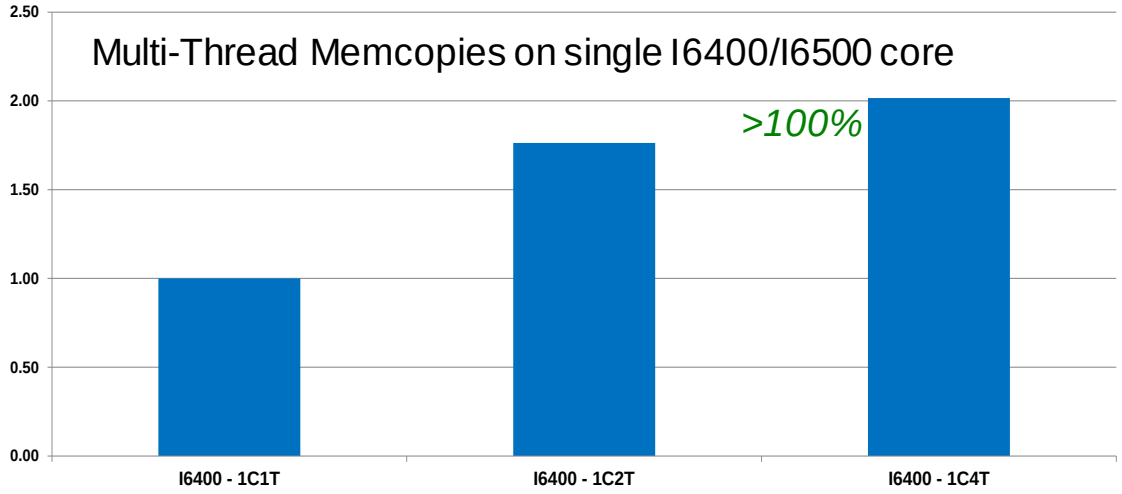
- A path to higher performance, and higher efficiency
- 30%-60% higher performance for 10% per Thread increase

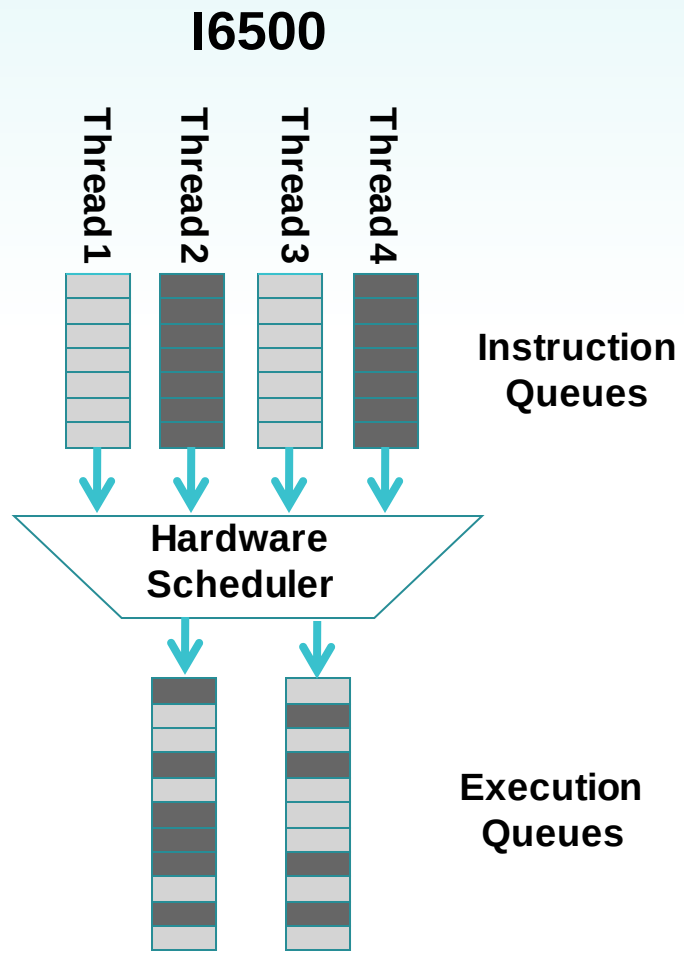
2 Easy to use – programming model is same as multi-core

- A thread looks like a core to standard SMP OS

3 Simultaneous / concurrent execution

- Zero Cycle overhead context switching





MIPS IP Cores – Mapping to ARM

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FPU	✓ (UC version only)	✓	-	MT	-	MT w/SIMD	Hi Perf w/SIMD	Hi Perf w/SIMD
DSP/SIMD extensions	DSP ASE r2	DSP ASE r2	DSP ASE r2	DSP ASE r2	DSP ASE r2	MSA 128-bit	MSA 128-bit	MSA 128-bit
Virtualization	-	✓	-	-	-	✓	✓	✓
Small code size ISA	microMIPS32	microMIPS32	microMIPS32	MIPS16e2 ASE	nanoMIPS32	-	-	-
Multi-threading	-	-	-	2 VPE, 9 TC	3 VPE, 9 TC	4 VPE	-	-
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SPRAMs (I/D/U)	✓ / ✓ / -	✓ / ✓ / -	✓ / ✓ / -	✓ / ✓ / -	✓ / ✓ / ✓	- / ✓ / -	- / - / -	- / - / -
L1 caches	✓	✓	✓	✓	✓	✓	✓	✓
L2 cache	-	-		✓	✓	✓	✓	✓
Coherent Multi-Core	-	-	-	Up to 4 cores	Up to 4 cores	Up to 6 cores, Up to 64 clusters	Up to 6 cores	Up to 6 cores
Native System Bus I/F	AHB-Lite	AHB-Lite	AXI	OCP 2 or AXI	AXI	AXI or ACE	AXI	AXI

Sample ARM Mapping

M3 M4 M23 M33 R52 R7 R8 A53 A57 A72

Thank You